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Design of Decimation Filters for Wireless Local Area Network Applications

Kantharaj S P*
BIET, Davangere, Karnataka, INDIA

G. S. Sunitha
BIET, Davangere, Karnataka, INDIA

G. H. Leela
BIET, Davangere, Karnataka, INDIA

S. O. Nirmala
BIET, Davangere, Karnataka, INDIA

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Abstract

Multirate signal processing is critical to realizing the digital frequency converter in WLAN technologies. In this paper, we focus on designing and analyzing the different structures of decimators that support WLAN-b applications to reduce the frequency by 12 for an IEEE. The structure modeling of the decimator used Simulink. Implementing a single-stage decimator required a higher-order filter, extra storage space, and a long simulation time. Results showed that the necessary storage elements for 2-stage design are 55% and for 3-stage design is 65% of single stage. For 133 MHz WLAN-b application, a two-stage decimator is proved to be efficient.

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INTRODUCTION

In many signal processing and communication applications, it is necessary to convert the audio signal at a given frequency to some other signals with different sampling rates. In digital audio, three different sampling rates are 32 kHz for broadcasting, 44.1 kHz for CD, and 48 kHz for digital audiotape. A wireless local area network (WLAN) uses a wireless distribution technique to two or more devices. It also allows users to shift around within a geographical local coverage area, connect to the network, and connect to the wider internet [1], [2].

Sample Rate Conversion (SRC) is a process by which the audio sample rate gets changed without affecting the audio pitch [3]. It is comfortable to design and analyze the implementation of transmultiplexer by multirate DSP systems [4]. The systems which operate at different sampling rates throughout the processing are called multirate systems. In multirate systems, the sampling frequency changes during signal processing [5]. Multirate systems have gained popularity since the early 1980s, and they are commonly used for audio and video processing, communications systems, and transform analysis, to name a few. Multirate systems play a central role in many areas of signal processing [6]. The primary operations of multirate systems are Decimation and Interpolation. Decimation and interpolation are the two basic building blocks of multirate digital signal processing systems [7]. Decimation reduces the sampling rate, whereas interpolation is used to increase the sampling rate [8].

In practice, decimation usually implies low pass-filtering of a signal, then throwing away some of its samples [9]. The most immediate reason to decimate is simply to reduce the sampling rate at the output of a system so the system operating at a lower sampling rate can input the signal [10]. The main task of a decimation filter is to remove the quantization noise away from the band of interest and avoid aliasing of high-frequency components down to the low-frequency region or within the signal bandwidth [11].

Corresponding author:
Kantharaj S P, Bapuji Institiute of Engineering and Technology, Davanagere-577004, India. ✉ kantharajsp@gmail.com

Khalid et al. presented the decimation filter simulated using Matlab, and its complete architecture was realized using DSP Blockset and Simulink. The filter was implemented using Mentor Graphic ModelSim and Calibre Tool in FPGA technology. The resulting architecture is hardware efficient and consumes less power than conventional decimation filters [12]. Jing showed that Compared with a conventional digital filter, the more efficient filter has a great advantage in the real-time and the use of hardware resources, which can improve the real-time performance of the signal processing and greatly reduce the rate of the back-end digital signal processing [13]. Kim also said that the complexity of the circuit is reduced by applying the required down-sampling rate twice instead of once. In addition, CIC decimation filters without a multiplier are used as the decimation filter of the first stage. The second stage is implemented using a CIC filter and a down sampler with an anti-aliasing filter, respectively [14]

Multirate signal processing is the key technology to realizing the digital frequency converter in WLAN technologies. For a wireless local area network, multirate systems perform a processing task with improved efficiency and offer higher performance at a lower cost and reduced complexity [15]. In this paper, we focus on designing and analyzing the different structures of decimators that support WLAN-b applications to reduce the frequency by 12 for an IEEE. The design is subjected to retaining the passband aliasing in the desired bounds.

METHOD

Sampling Rate Conversion

The sampling rate change may be achieved in one fell swoop or multi fell swoops. Sampling rate conversion by integer factors in a single stage is useful but can be too restrictive in some practical applications [16]. The structure modeling of the decimator used Simulink. Implementing a single-stage decimator requires a higher-order filter, extra storage space, and a long simulation time. The multistage design approach has advantages over the single-stage sampling rate converters. In a multistage structure, the conversion factor is translated into a product of integer values such that conversion can be carried out in more than one stage. But no systematic approach is formulated in the literature to determine the optimal number of stages and factors to minimize storage space and computation time. The trial-and-error method may mostly be applied for such designs [17], [18].

For sampling rate converters, additional efficiency is achieved by cascading two or more stages design. Depending upon the application and the required response, a suitable filter and design method can be adopted for frequency conversion in the case of WLAN. This paper uses symmetric Linear FIR filters designed by the optimal method for sampling rate converters because of their advantages [19]. In WLAN applications, frequency converter system performance can be enhanced by simplifying arithmetic operations determined by the number of multiplications per sample and the number of total storage elements [20].

RESULTS AND DISCUSSION

Structure Modelling of Decimator Using Simulink

In this paper, we focus on designing and analyzing the different structures of decimators that support WLAN-b applications. For interoperating between two WLAN-b's, consider designing the decimator to down-convert 132 MHz frequency input signal to 11 MHz as specified in table 1.

Table 1. Design Specification for WLAN Application.

Specifications	Values
Input sampling frequency	132 MHz
Output frequency	11 MHz
Pass band frequency	3 MHz
Stop band frequency	5 MHz
Frequency deviation	0.015
Pass band attenuation	0.5 db
Stop band attenuation	44 db

Single-stage implementation

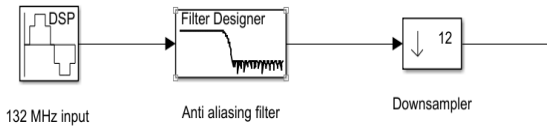

Figure 1. Block Modelling of Single Stage Decimator.

The sampling rate reduction required for WLAN is 12, which is realized with a single stage and multistage decimator structure. To compare performances, the decimator is designed using the above specifications as a single stage and multistage structure. We have implemented the same using MatLab Simulink. These structures' performance metrics like MPS and TSR are evaluated and compared. In one fell swoop design, the decimator consists of an anti-aliasing filter followed by a 12-fold down sampler, as shown in figure 1. Decimator specifications are listed in table 2.

Table 2. Single Stage Decimator Specifications.

Specifications	Values
Input sampling frequency	132 MHz
Decimation Factor	12
Pass band frequency	3 MHz
Stop band frequency	5 MHz
Frequency deviation	0.015
Pass band attenuation	0.5 db
Stop band attenuation	44 db
Order	101
Multiplications (in terms of 106)	1100
Storage Elements	101

Two-stage decimator implementation

Figure 2 shows a two-stage structure for the down sampling. In the two-stage decimator model, sampling rate reduction factor 12 is considered M1 x M2 (possibly as 4x3 and 3x4). The design aspects and performance measures of two-stage decimators are listed in table 3.

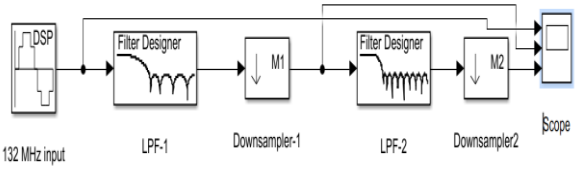

Figure 2. Block Modelling of Two Stage Decimator.

Three-stage decimator implementation

In 3-stage approach, the decimation factor 12 is factorized as M1 x M2 x M3 (possibly as 4x2x2, 2x4x2 and 2x2x4). Figure 4 shows the three-stage structures for the rate conversion. Table 3 shows the performance measures of three-stage decimators for converting 132MHz signal to 11MHz signal. Decimator design computational efficiency can be analyzed based on the number of multiplications per input sample and the number of delay elements required to perform the sampling rate conversion of WLAN-b.

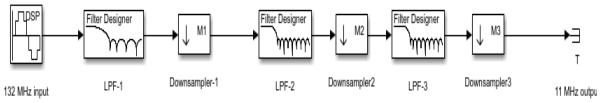

Figure 3. Block Modelling of Three Stage Decimator.

Tables 2, 3, and 4 show the multiplications and number of storage elements (number of delay elements which are the same as storage elements) required. We believe that reducing the number of filters reduces the complexity involved in designing the decimators. Results show that the required storage elements for 2-stage design are 55% and for 3-stage design is 65% of single stage. For multistage decimators in WLAN-b, the better approach to finding the optimal number of stages and set of integers is apropos computational complexity and total storage requirements. To the specified WLAN-b application, two stages decimator is appeared to be the most efficient in the dimension of the number of multiplications and storage elements. More precisely, to achieve better performance during the multistage decimator design, it is good to choose the largest integer of all the possible factors of M as M1.

Table 3. Two Stage Decimator Specifications

Two stage decimator				
Parameters	Factors: M1=4, M2=3		Factors: M1=3, M2=4	
Input frequency	132 MHz	33 MHz	132 MHz	44 MHz
Pass band frequency	3 MHz	3 MHz	3 MHz	3 MHz
Stop band frequency	27.5 MHz	5.5 MHz	38.5 MHz	5.5 MHz
Frequency deviation	0.18	0.075	0.27	0.045
Pass band attenuation	0.006	0.006	0.006	0.006
Stop band attenuation	0.05	0.05	0.05	0.05
Order	11	33	7	43
Multiplications (in terms of 10^6)	583		737	
Storage Elements	44		50	

Table 4. Three Stage Decimator Specifications

Parameters	Factors: M1=3, M2=2, M3=2			Factors: M1=2, M2=3, M3=2			Factors: M1=2, M2=2, M3=3		
Input frequency	132 MHz	44 MHz	22 MHz	132 MHz	66 MHz	22 MHz	132 MHz	66 MHz	33 MHz
Pass band frequency	3 MHz	3 MHz	3 MHz	3 MHz	3 MHz	3 MHz	3 MHz	3 MHz	3 MHz
Stop band frequency	38.5 MHz	16.5 MHz	5.5 MHz	60.5 MHz	16.5 MHz	5.5 MHz	60.5 MHz	27.5 MHz	5.5 MHz
Frequency deviation	0.26	0.3	0.11	0.43	0.2	0.11	0.43	0.35	0.07
Pass band attenuation	0.016	0.016	0.016	0.016	0.016	0.016	0.016	0.016	0.016
Stop band attenuation	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
Order	7	6	23	7	9	21	5	5	25
Multiplications (in terms of 10^6)		693			891			770	
Storage Elements		36			37			35	

CONCLUSION

Symmetric linear phase FIR filters designed by the optimal method are used to design the decimator. Results show the multistage designs yield significant reductions in computation speed and storage requirements compared with single-stage designs. For 133 MHz WLAN-b application, a two-stage decimator is proved to be efficient.

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