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The Performance Multilevel Inverter 5 Level 1 Phase by Reducing Power Switch Components

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A B S T R A C T

Multilevel Inverter (MLI) is a converter that converts DC power source into AC power source with voltage output more than 2 levels. The conventional 5-level Multilevel Inverter Topology that is developing today generally uses eight power switch components. In this paper, research Topology multilevel inverter 5 levels was conducted by reducing the power switch components into four pieces and assisted by two diode clamps and capacitor as voltage coupling. PWM (Pulse Width Modulation) technique used to utilize multicarrier modulation. Simulation testing with MATLAB conducted has been verified with the results of hardware tests where the output voltage shows similarity of shape at the output voltage MLI 5 levels. The results and discussion of the proposed topology can provide economic benefits from the use of the number of power switch components (MOSFET) compared to conventional 5-level MLI topology.

INTRODUCTION

The development of power electronics makes it possible to produce efficient and economical generation, processes and use of electrical energy. Power electronics are defined as electronic applications that focus on the regulation of electrical equipment by changing electrical parameters (current, voltage, frequency and electric power). Nowadays, Multilevel Inverter has attracted great interest in the high power industry, with the various advantages of this widely applied power electronics equipment such as: DC Resource Utilization, Uninterruptible Power Supplies, Direct Voltage Power Transmission (HVDC), variable frequency drive system, Air Conditioner and others[1].

Multilevel Inverter (MLI) is a converter that converts a DC power source into an AC power source where the output form of voltage is more than two levels (three levels, five levels, seven levels and etc). Many output levels can be set with some semiconductor switches on the power circuit. The growing Multilevel Inverters can be recognized based on their architecture (topology) such as diode clamped, flying capacitor and cascade H-bridge. They are three multilevel inverter structures known in industrial applications with separate DC sources. The advantage of diode clamped and flying capacitor is these two use a voltage balancer with a capacitor, so that for many voltage levels at DC sources it can be minimized [2]–[7].

Conventional 5-level MLI requires eight switches to split two DC sources separately [7]. The next 5-level of MLI topology are widely proposed techniques and methods in reducing the number of components used [8]–[12]. In this research, we designed a multilevel 5-level inverter using four switches to chop two DC sources at positive polarity and negative polarity assisted by two clamp diodes and capacitors as voltage couplings[13], to analyze the harmonics produced by PWM (Pulse Width Modulation) techniques used to make use of multicarrier modulation. According to the obtained result, the proposed topology can reduce the cost and amount of components used in the existing Topology.

Table 1. Components of MLI 5 level

Type of MLI	Number of power switch	Number of diode	Number of capacitor
Dioda Clamped	8	12	4
Flying Capacitor	8	-	10
Cascade H-bridge	8	-	-
[4]	6	-	2
[5]	5	4	-
[6]	8	-	3
[7]	5	1	2
[8]	5	1	-
Proposed design	4	2	2

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MLI 5 LEVEL TOPOLOGY

The development of MLI topology 5 levels is currently widely done in reducing the number of components in conventional MLI, validation of the number of components used is shown in table 1.

METHOD

Proposed Topology

The proposed topology on a multilevel five-tier inverter was built using two DC sources, four power switch components, two diodes and two capacitors. The proposed set of topological power is shown in figure 1.

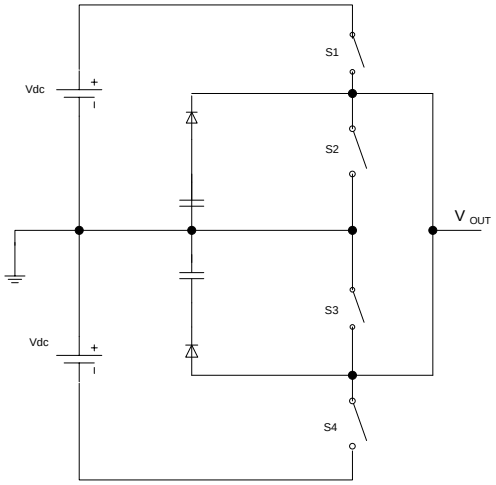


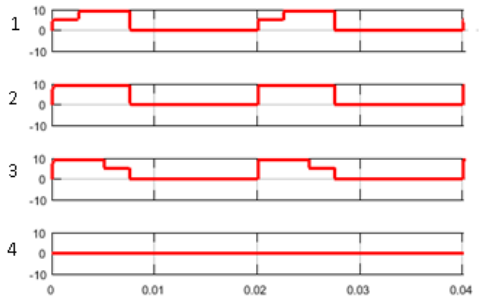
Figure 1. Topology MLI 5 Level

From figure 1, it can be explained the work of the proposed Topology where there are two DC sources at the upper limit and at the lower limit, the upper limit DC source is used for positive cycle polarity while the lower limit DC source is used for negative cycle polarity [14]. The two capacitors are used as couplings at voltage levels from large DC sources, while two diodes are used as clamps from each DC source. The proposed topology for power switch components is shown in table 2 below.

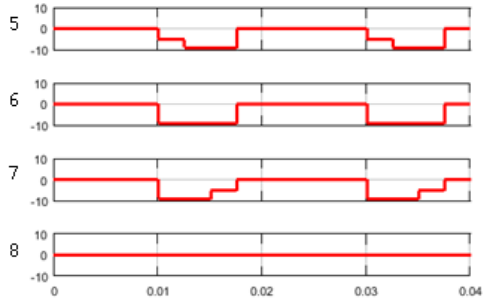
Table 2. Topology of switches MLI 5 level

condition	Existing condition of Switches				Output voltage
	S1	S2	S3	S4	
1	1	0	1	0	1/2 Vdc
2	1	0	0	0	Vdc
3	1	1	0	0	1/2 Vdc
4	0	1	0	0	0 Vdc
5	0	1	0	1	-1/2 Vdc
6	0	0	0	1	-Vdc
7	0	0	1	1	-1/2 Vdc
8	0	0	1	0	0 Vdc

To describe the output of the five topological levels proposed in figure 1, the model of positive cycle operation and negative cycle of the output voltage waves of each power circuit condition are shown in figure 2 below.



a. Positive Cycle



b. Negative Cycle

Figure 2. Output Voltage Operation Model (a) Positive Cycle, (b) Negative Cycle

From figure 2, it illustrates that the output voltage wave between the positive cycle condition and the negative cycle on the power circuit produces a five-level output as shown in figure 3 below.

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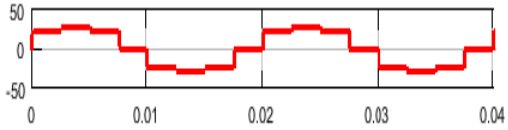

Figure 3. Output voltage of MLI 5 level

Pulse Width Modulation (PWM)

To obtain PWM waves, first generate reference waves (Vreference) and carrier waves (Vcarrier) [16]– [21], then both waves are compared to form the following reasoning model:

a. If Vreference > Vcarrier, then the pulse is produced in turning on conditions.
b. If Vreference < Vcarrier, then the resulting pulse is turning off condition

Figure 4 below shows the process of generating PWM waves.

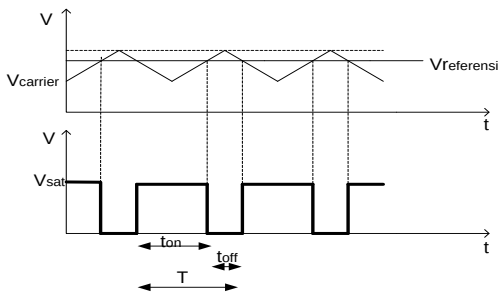

Figure 4. PWM Process

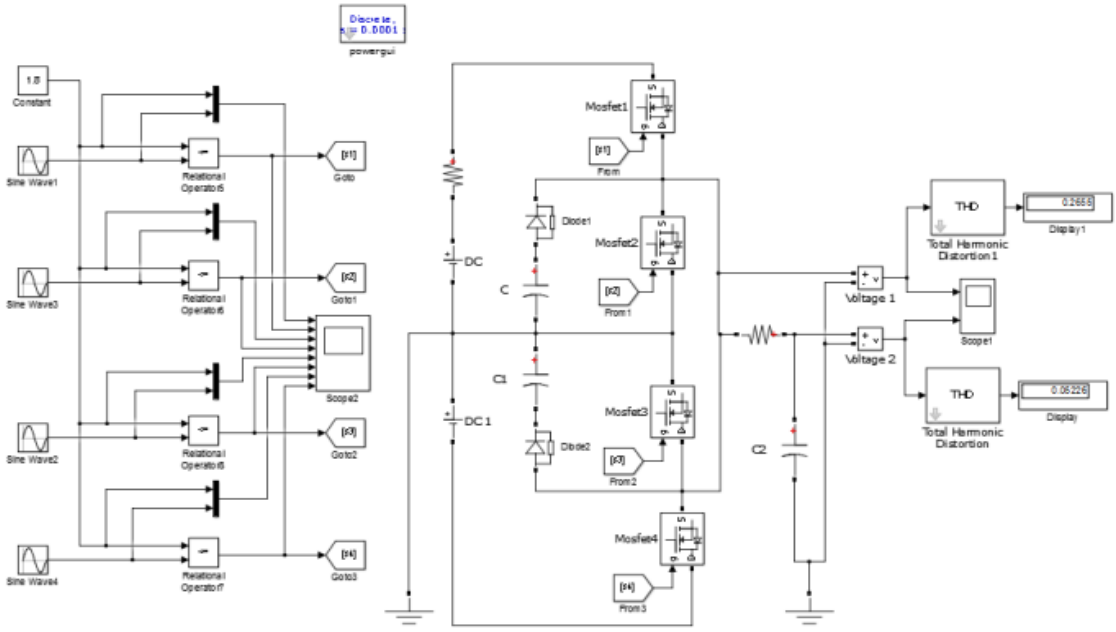

Figure 5. Simulation Model of MATLAB MLI 5 Level

$$D = \frac{t_{on}}{(t_{on}+t_{off})} \quad (1)$$

Total Harmonic Distortion (THD)

Previous researches of MLI technology have been done to obtain MLI 5-level output voltage. The main technology in developing Multilevel Inverter is how to modify the pattern of output level approaching sinusoidal waves. With a fourier series, the harmonic components are expressed in the following equation:

$$V_0(\omega t) = V_0 + \sum_{n=1}^{\infty}(a_n \sin n\,\omega t) + \sum_{n=1}^{\infty}(b_n \cos n\,\omega t) \quad (2)$$

THD represents the magnitude of distortion or deviation of a wave containing harmonics expressed in percent (%) formulated as follows:

$$THD = \frac{\sqrt{V^2{}_{2(rms)} + V^2{}_{3(rms)} + V^2{}_{4(rms)} + \cdots + V^2{}_{n(rms)}}}{V_{1(rms)}} \quad (3)$$

$$= \frac{\sqrt{V^2{}_{rms} - V^2{}_{1(rms)}}}{V_{1(rms)}} \quad (4)$$

where:

$V_{1(rms)}$ = effective voltage harmonic base

$V_{n(rms)}$ = harmonic effective voltage to – n

As shown in figure 5, the each of DC source used has a voltage of 12 Volts that will be chopped into 5-level MLI output. For PWM wave generation is by comparing sine waves (Vreference) to DC waves (Vcarrier), the process of generating PWM waves is shown in figure 6 and the pattern of output voltage is shown in figure 7.

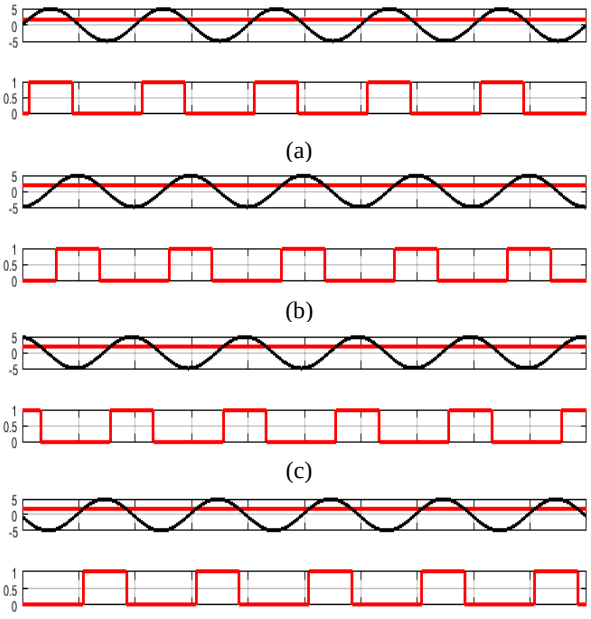

Figure 6. PWM Process, (a) S1 (b) S2 (c) S3 (d) S4

In Figure 6, it can be seen that PWM produced is S1 and S2 having a delay due to the phase shift of sine waves (Vreferensi) of 120^0. This phenomenon was similar to S3 and S4. The PWM switching pattern is used to chop the voltage source input from the proposed 5-level MLI topology.

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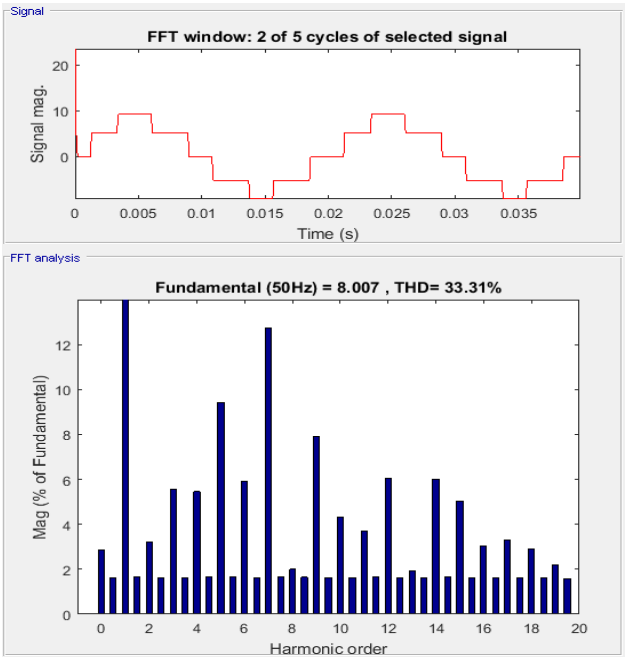

Figure 7. MLI Output 5 Levels

MATLAB simulation results that have been done large amplitude voltage obtained by 10 Volts, while the input of the source voltage of 12 Volts then drop the output voltage amplitude based on the input of dc source voltage by 16%, and a large harmonic output voltage of 33.31%. From several previous studies for MLI 5 large levels of harmonic voltage were obtained 31.70%[7], 35.19%[12], 35.51%[2], respectively. therefore it is necessary to conduct hardware testing as proof of the characteristics of the proposed 5-level MLI topology.

EXPERIMENT

In the proposed MLI topology hardware testing, the circuit requirements used were sine wave generation circuits, function generators, DC regulators, comparators, gate drivers, MOSFET and using two 6.5V batteries. The battery is a power source which was chopped as wave pattern into a multilevel inverter output. A series of hardware performances in this study are shown in figure 8.

RESULTS AND DISCUSSION

Simulink Model

In this study, proposals were discussed using PWM techniques. Figure 5 below shows the 5-level MATLAB MLI simulation model.

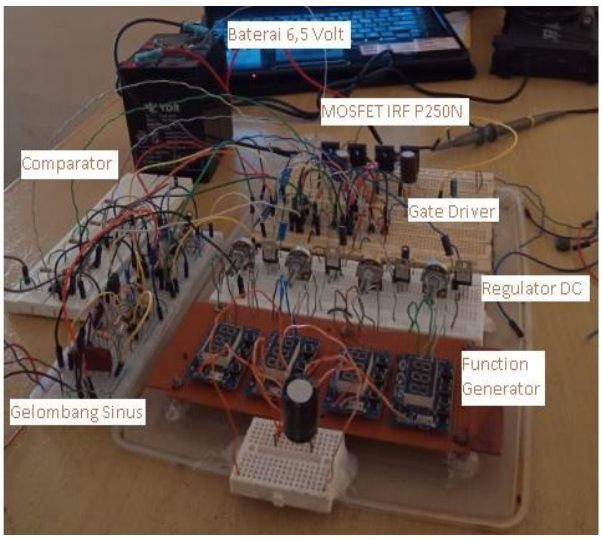

Figure 8. Series of MLI 5-Level Performance

PWM Generation Process

As described in figure 8, sine wave generation (Vref) uses IC LM 358 with a frequency setting of 50.2 Hz and the amplitude of 10 Volts, while the carrier wave generation (Vcarrier) uses a DC regulator with the voltage amplitude of 1.8 Volts. To compare these two waves in producing PWM waves, it needed IC Comparator LM 393, as for duty cycle produced by IC Comparator by 37.7% and frequency 50 Hz. Figure 9 shows the process of generating PWM process, while the PWM waves pattern was showed in figure 10.

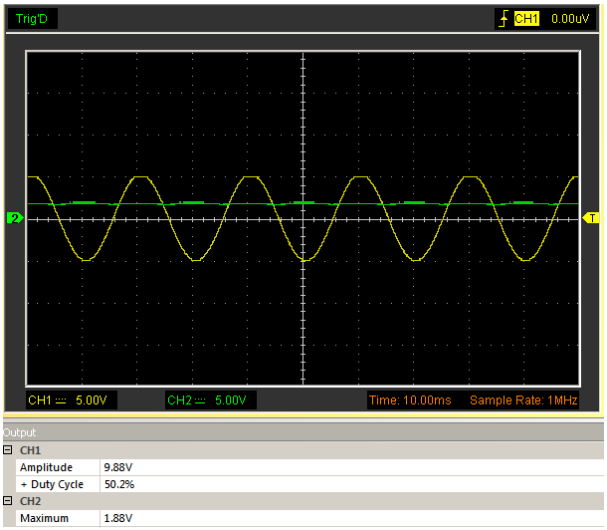

Figure 9. PWM Process

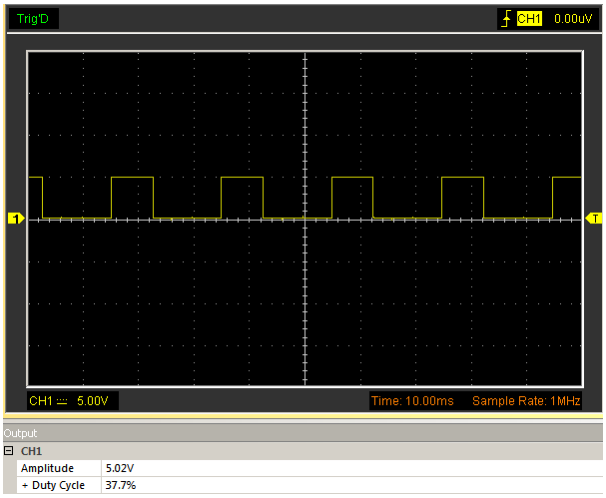

Figure 10. PWM Waves

Testing of Gate Driver MOSFET

To chop the battery DC input voltage on the proposed MLI topology power circuit, the PWM waves as the dissolving of 4 MOSFET components each have the similar duty cycle size and have a delay difference of 2.5 ms at a frequency of 50 Hz. As developed by F.F and M.I Hamid [15], to avoid the heat effect on the MOSFET the backflow at the time of signaling does not result in a heat effect, the output of PWM waves is made isolated from the system. The pattern of gate driver for each MOSFET (S1, S2, S3 and S4) was showed in a row in figure 11 and figure 12.

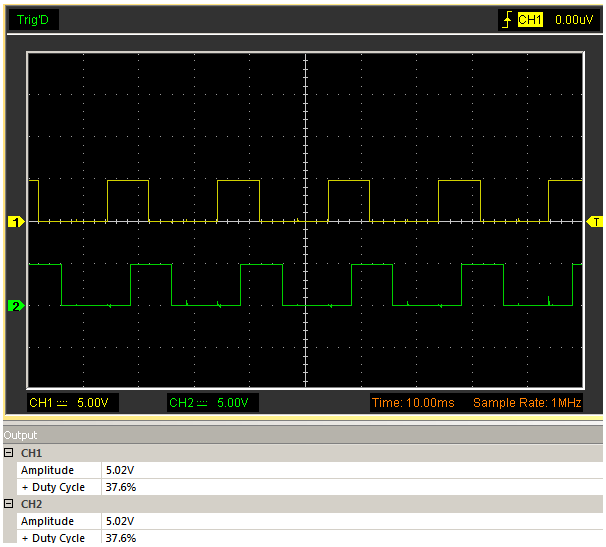

Figure 11. Gate Driver S1 and S2

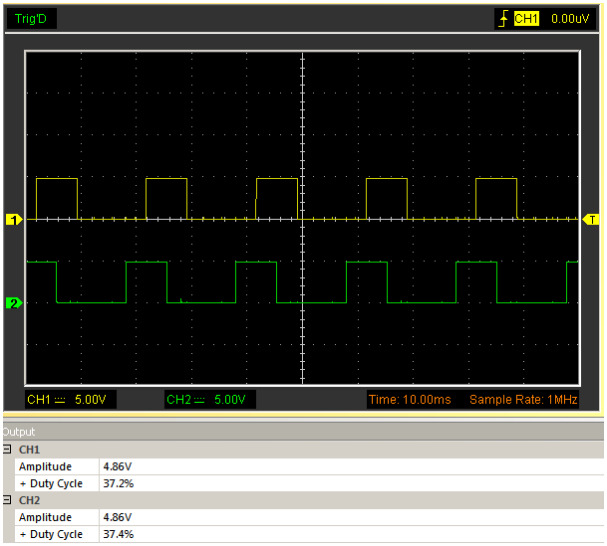

Figure 12. Gate Driver S3 and S4

MLI 5 Level

After obtaining the MOSFET gate driver, testing and measurement on the proposed 5-level MLI topology was done. The topology MLI - 5 level is a type of MOSFET IRFP 250N as power switch component. The hardware testing shown in figure 13 and the results of hardware performance measurements for MLI 5 levels that have been performed are shown in figure 14.

Figure 13. Hardware testing

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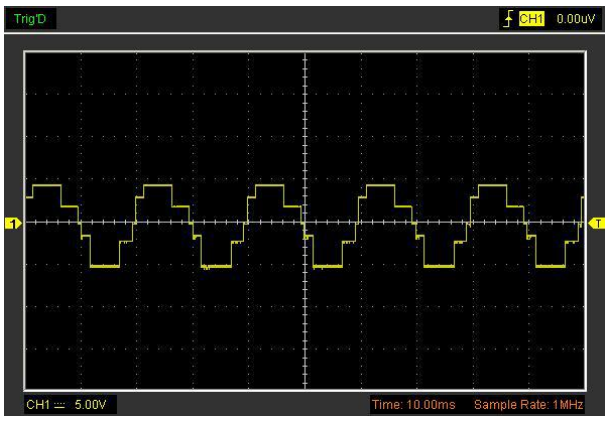

Figure 14. MLI 5 Level

According to the results of the proposed 5-level MLI experiment, which is illustrated in figure 14, decreased the input voltage 6 volts to be output voltage 5 volts. It can be concluded that the decreasing of amplitude voltage is 16.6%.

CONCLUSIONS

Matlab Simulation Results that have been conducted similar pattern of output voltage MLI 5 levels have been experimentally verified and similar results have been obtained. The characteristic topology of conventional 5-level MLI has a total of eight power switch components, with the proposed 5-level MLI topology able to reduce the number of power switch components using only four pieces. The results and discussion of the proposed topology can provide an economic advantage from the use of the number of power switch components (MOSFET).

REFERENCES

[1] N. Devarajan and A. Reena, "Reduction of Switches and DC Sources in Cascaded Multilevel Inverter," *Bull. Electr. Eng. Informatics*, vol. 4, no. 3, pp. 186–195, 2015, doi: 10.11591/eei.v4i3.501.

[2] R. Hemanthakumar, V. Raghavendrarajan, C. S. Ajin Sekhar, and M. Sasikumar, "A novel hybrid negative half cycle biased modulation scheme for cascaded multilevel inverter," *Int. J. Power Electron. Drive Syst.*, vol. 4, no. 2, pp. 204–211, 2014, doi: 10.11591/ijpeds.v4i2.5696.

[3] D. Roy, S. Kumar, and M. Singh, "A novel region selection approach of SVPWM for a three-level NPC inverter used in electric vehicle," *Int. J. Power Electron. Drive Syst.*, vol. 10, no. 4, p. 1705, 2019, doi: 10.11591/ijpeds.v10.i4.pp1705-1713.

[4] H. Behbahanifard, S. Abazari, and A. Sadoughi, "New scheme of SHE-PWM technique for cascaded multilevel inverters with regulation of DC voltage sources," *ISA Trans.*, vol. 97, no. xxxx, pp. 44–52, 2020, doi: 10.1016/j.isatra.2019.07.015.

[5] A. Mohamed and S. Salimin, "Thd performance of single phase five level inverter using proportional resonant and harmonic compensators current controller," *Int. J. Power Electron. Drive Syst.*, vol. 11, no. 3, pp. 1423–1429, 2020, doi: 10.11591/ijpeds.v11.i3.pp1423-1429.

[6] G. V. V. Nagaraju and G. S. Rao, "Three phase PUC5 inverter fed induction motor for renewable energy applications," *Int. J. Power Electron. Drive Syst.*, vol. 11, no. 1, pp. 1–9, 2020, doi: 10.11591/ijpeds.v11.i1.pp1-9.

[7] M. Khanfara, R. El Bachtiri, M. Boussetta, and K. El Hammoumi, "A Multicarrier PWM Technique for Five Level Inverter Connected to the Grid," *Int. J. Power Electron. Drive Syst.*, vol. 9, no. 4, p. 1774, 2018, doi: 10.11591/ijpeds.v9.i4.pp1774-1783.

[8] P. Thongprasri, "A 5-Level Three-Phase Cascaded Hybrid Multilevel Inverter," *Int. J. Comput. Electr. Eng.*, vol. 3, no. 6, pp. 789–794, 2011, doi: 10.7763/ijcee.2011.v3.421.

[9] N. A. Yusof, N. M. Sapari, H. Mokhlis, and J. Selvaraj, "A comparative study of 5-level and 7-level multilevel inverter connected to the grid," *PECon 2012 - 2012 IEEE Int. Conf. Power Energy*, no. December, pp. 542–547, 2012, doi: 10.1109/PECon.2012.6450273.

[10] K. Karthik, B. L. Narsimharaju, and S. S. Rao, "Five-level inverter using POD PWM technique," *Int. Conf. Electr. Electron. Signals, Commun. Optim. EESCO 2015*, 2015, doi: 10.1109/EESCO.2015.7254048.

[11] R. Rasheed, S. K K, and B. V, "A five-level multilevel topology utilizing multicarrier modulation technique," *Int. J. Power Electron. Drive Syst.*, vol. 10, no. 2, p. 868, 2019, doi: 10.11591/ijpeds.v10.i2.pp868-873.

[12] K. Janardhan, A. Mittal, and A. Ojha, "Performance investigation of stand-alone solar photovoltaic system with single phase micro multilevel inverter," *Energy Reports*, vol. 6, pp. 2044–2055, 2020, doi: 10.1016/j.egyr.2020.07.006.

[13] N. MOHAN, *Book*, 1st ed., vol. 1. USA: Don Fowley, 2012.

[14] H. Matalata and V. Yusiana, "New Topology Multilevel Inverter Type Diode Clamped Five Level Single Phase," *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 807, no. 1, 2020, doi: 10.1088/1757-899X/807/1/012039.

[15] . F. and M. I. Hamid, "Desain Rangkaian Gate-Driver untuk Konverter yang Bekerja dengan Voltage Mode Control," *J. Nas. Tek. Elektro*, vol. 5, no. 2, p. 175, 2016, doi: 10.25077/jnte.v5n2.259.2016.

[16] H. Nazif and M. I. Hamid, "Pemodelan Dan Simulasi PV-Inverter Terintegrasi Ke Grid Dengan Kontrol Arus 'Ramp Comparison Of Current Control,'" *J. Nas. Tek. Elektro*, vol. 4, no. 2, p. 129, 2015, doi: 10.25077/jnte.v4n2.139.2015.

[17] H. Matalata and M. I. Hamid, "Pengembangan Topologi Inverter Multilevel Tiga Tingkat Satu Fasa Tipe Dioda Clamped dengan Mereduksi Komponen Saklar Daya," *J. Nas. Tek. Elektro*, vol. 5, no. 3, p. 360, 2016, doi: 10.25077/jnte.v5n3.314.2016.

[18] B. Chokkalingam, M. S. Bhaskar, S. Padmanaban, V. K. Ramachandaramurthy, and A. Iqbal, "Investigations of multi-carrier pulse width modulation schemes for diode free neutral point clamped multilevel inverters," *J. Power Electron.*, vol. 19, no. 3, pp. 702–713, 2019, doi: 10.6113/JPE.2019.19.3.702.

[19] S. Edwin Jose and S. Titus, "A level dependent source concoction multilevel inverter topology with a reduced number of power switches," *J. Power Electron.*, vol. 16, no. 4, pp. 1316–1323, 2016, doi: 10.6113/JPE.2016.16.4.1316.

[20] R. A. Rana, S. A. Patel, A. Muthusamy, C. W. Lee, and H. J. Kim, *Review of multilevel voltage source inverter topologies and analysis of harmonics distortions in FC-MLI*, vol. 8, no. 11. 2019.

[21] R. Palanisamy *et al.*, "Simulation of single phase 3-level Z-source NPC inverter with PV system," *Telkomnika (Telecommunication Comput. Electron. Control.*, vol. 16, no. 5, pp. 2293–2301, 2018, doi: 10.12928/TELKOMNIKA.v16i5.7098.

 https://doi.org/10.25077/jnte.v10n2.831.2021