

## Optimal design of a single-phase APF based on PQ theory

Dur Muhammad Soomro<sup>1</sup>, S. K. Alswed<sup>2</sup>, Mohd Noor bin Abdullah<sup>3</sup>, Nur Hanis binti Mohammad Radzi<sup>4</sup>, Mazhar Hussain Baloch<sup>5</sup>

<sup>1,2,3,4</sup> Department of Electrical Power Engineering, FKEE, Universiti Tun Hussein Onn Malaysia, Malaysia

<sup>5</sup> Department of Electrical Engineering, Mehran University Engineering SZAB Campus Khairpur, Pakistan

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### ABSTRACT

The instantaneous active and reactive power (PQ) theory is one of the most widely used control theory for shunt active power filter (SAPF), which can be implemented in single-phase and three-phase systems. However, the SAPF with PQ theory still had ability to improve to become more efficient. This paper presents the optimal design of a single-phase SAPF in terms of reducing the current harmonic distortion and power loss in voltage source inverter (VSI) controlled with the semiconductor switching devices IGBT, MOSFET and Hybrid (combination of IGBT and MOSFET). In order to reduce the switching frequency and power loss of VSI, instead of using single-band hysteresis current controller (HCC), double-band HCC (DHCC) and triple-band HCC (THCC) is used in the SAPF. The designed SAPF is tested with different non-linear loads to verify the results by using MATLAB Simulink.

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### Corresponding Author:

Sager K. Alswed,

Department of Electrical Power Engineering,

Universiti Tun Hussein Onn Malaysia,

86400 Batu Pahat, Johor, Malaysia.

Email: ge140016@siswa.uthm.edu.my

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## 1. INTRODUCTION

The increasing human population results in an increased demand for electricity. Since most of the electricity is generated by fossil fuel which is depleting day by day and causing air pollution. In order to overcome this crisis, energy efficiency equipment (EEE), electrical vehicles (EV) and renewable energy (RE) like solar and wind power are introduced. However, the mentioned solution is able to reduce the power consumption but will increase the harmonic in power system (PS) [1]. This is due to the EEE, the charging of EV and usage RE that requires the use of the semiconductor switching devices such as converters, which will drag the current to non-linearly form, thus causes harmonic injection in the PS. These loads are known as non-linear loads, which are the source of harmonic in PS.

The effect of harmonic will cause malfunction of sensitive electronic loads, malfunction of protection devices and power loss in the PS [2-3]. Therefore, people have more concern to improve PS quality. Among many other harmonic mitigation methods, SAPF is one of the most effective methods to deal with PS harmonic [4]. Besides harmonic compensation SAPF is also able to improve the power factor (PF), reduce the neutral current and unbalanced current condition.

Among other control theories for SAPF, the PQ theory is the most popular control theory used by the researchers [5]. This is due to the reason that PQ theory is able to give instantaneous harmonic compensation with fast response and applicable to single-phase as well as a three-phase system. Usually the PQ theory will pair with the HCC to give the fast response with a simple design. However, the normal HCC will produce high-frequency switching and will cause higher switching loss for the inverter. Therefore,

in order to overcome the mentioned problem, DHCC and THCC are proposed [6]. Literature review shows that using DHCC and THCC able to reduce the switching frequency [7]. The advantages of reducing the switching frequency are able to reduce the switching stress and reduce the switching loss of the inverter.

This paper presents optimal design of single-phase SAPF with PQ theory, and the performance observed with HCC, DHCC and THCC for low voltage application by using MATLAB Simulink. To validate the proposed design of SAPF is tested on 5 types of non-linear loads. This paper also included the optimal design of SAPF in terms of the selection of the semiconductor switching devices for the VSI, dc-link capacitor ( $C_{DC}$ ) and coupling inductor ( $L_{APF}$ ).

## 2. RESEARCH METHODOLOGY

### 2.1 Deign of the filter

There are various types of control theories that handle power filter applications [8]. However, for practical applications, power filter depends on more than just control theories but also design parameters values of  $C_{DC}$  and  $L_{apf}$ . They play a significant role in ensuring successful operation of SAPF.

In this paper, SAPF topology is implemented to optimize and reduce current harmonics. The configuration of SAPF in PS is shown in Figure 1. The VSI is implemented in the SAPF and connected with a  $C_{DC}$  to provide needed reactive power to compensate for current harmonics. Incorporated switching devices in VSI utilize semiconductors such as GTO [9], MOSFET [10] or IGBT [11], to provide switching pulses based on calculated harmonic compensation current ( $I_{comp}$ ) according to control theory. The  $L_{APF}$  is connected in series with SAPF to mitigate harmonics ripple effect by compensating reactive current. In the following detailed explanation of control theory, the determination of  $C_{DC}$  and  $L_{APF}$  values for VSI SAPF is provided.

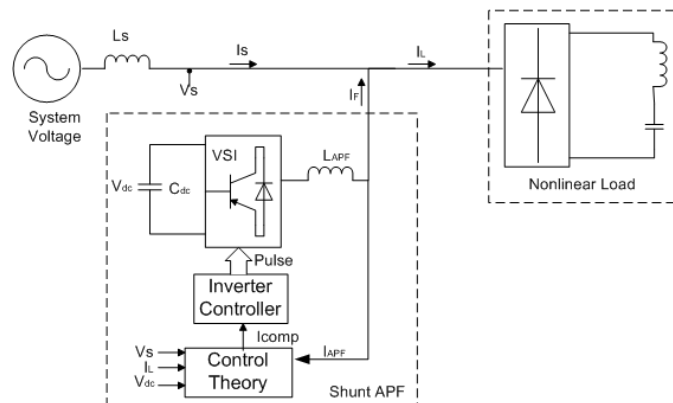


Figure 1. Connection of SAPF in PS

In order to verify the performance of the designed SAPF model, tested with different types of non-linear loads were performed.

### 2.2 Control theory – instantaneous active and reactive power (PQ) theory

PQ theory was firstly introduced by Hirofumi Akagi to define instantaneous power for three-phase circuits in the time domain [12]. This control theory is modified to be applied in three-phase four wires system and single-phase system [13]. The calculation of the active power ( $P$ ) and reactive power ( $Q$ ) were based on instantaneous source voltage ( $V_{abc}$ ) and ( $I_{Labc}$ ) load current in three-phase PS [14]. Besides, it is also valid for steady-state or transient operation. Figure 2 shows the principal block diagram of the PQ theory. This control method is widely used due to its fast dynamic response against harmonics current compensation, system PF improvement, and unbalanced current loads conditions enhancement [15]. However, it requires an accurate and balanced sinusoidal source voltage. Therefore, for unbalanced and distorted source voltage condition a Unit Vector Template (UVT) addition is needed [16] or PLL with PQ theory.

In order to use the PQ theory for the single-phase system, firstly, it needs to transform single-phase supply voltage and non-linear load current from  $V_S$  and  $I_L$  to imaginary three-phase  $V_{abc}$  and  $I_{Labc}$  form respectively. Both imaginary  $v_{abc}$  and  $i_{Labc}$  signals will be sent to Clarke's Transformation to transform from  $abc$  plane into  $\alpha\beta 0$  coordinates as follows:

$$\begin{pmatrix} v_0 \\ v_\alpha \\ v_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix} \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \tag{1}$$

$$\begin{pmatrix} i_0 \\ i_\alpha \\ i_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix} \begin{pmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{pmatrix} \tag{2}$$

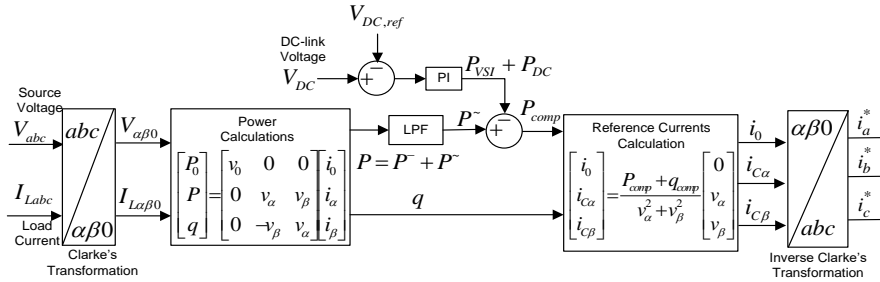


Figure 2. Principal block diagram of PQ theory

The PQ theory treats the three-phase system as a unit. The calculation of instantaneous P and Q is based on  $\alpha\beta 0$ -coordinates, voltages and currents. Calculated instantaneous power is defined as instantaneous zero sequence power ( $P_0$ ), P and Q. Besides, the calculated  $P$  is the total active power of the system, including the power used by the load known as dc-component (fundamental component or active power,  $\bar{P}$ ) and the ac-component (harmonic power,  $\tilde{P}$ ). Therefore, it can be written as:

$$P = \bar{P} + \tilde{P} \tag{3}$$

The low pass filter (LPF) is used to filter out the  $\tilde{P}$  to retain only the  $\bar{P}$ . This  $\tilde{P}$  signal represents the harmonic power. The power loss in SAPF contain power loss in VSI ( $P_{VSI}$ ) and power loss in  $C_{DC}$  ( $P_{DC}$ ) which can be expressed as:

$$P_{PF} = P_{VSI} + P_{DC} \tag{4}$$

The  $P_{VSI}$  value depends on the types of semiconductor switching devices and the switching frequency ( $f_{sw}$ ).  $P_{VSI}$  was explained in detail previously in the “selection of the switching devices for the SAPF” section. The  $P_{DC}$  can be obtained by using Proportional Integral (PI) controller as a result of the error between the reference voltage ( $V_{DC,ref}$ ) and the measured DC-link voltage ( $V_{DC}$ ) as shown in (10).

$$P_{DC} = k_P(V_{DC,ref} - V_{DC}) + k_i \int (V_{DC,ref} - V_{DC}) dt \tag{5}$$

Thus, the compensation power ( $P_{comp}$ ) for the SAPF can be calculated by:

$$P_{comp} = (\bar{P} + P_{APF}) - P = (P_{VSI} + P_{DC})\tilde{P} \tag{6}$$

The reactive power compensation ( $q_{comp}$ ) is equal to the calculated Q. Thus, the  $\alpha\beta$  compensation reference currents are:

$$\begin{bmatrix} i_{Ca} \\ i_{Cb} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} P_{comp} \\ q_{comp} \end{bmatrix} \tag{7}$$

These compensation currents need to transform back to  $abc$  plane with Inverse Clarke’s Transformation as (8) and (9):

$$\begin{bmatrix} i_{Ca}^* \\ i_{Cb}^* \\ i_{Cc}^* \end{bmatrix} = \sqrt{2}/3 \begin{pmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{pmatrix} \begin{pmatrix} -i_0 \\ i_{c\alpha} \\ i_{c\beta} \end{pmatrix} \quad (8)$$

$$i_{Ca}^* = -\frac{1}{\sqrt{3}}i_0 + i_{c\alpha} = -\frac{1}{\sqrt{3}}i_0 + \frac{v_{\alpha}^*P_{comp} + v_{\beta}^*q_{comp}}{v_{\alpha}^2 + v_{\beta}^2} \quad (9)$$

For single-phase system, only the  $i_{Ca}^*$  signal from (9) is used to generate the switching pulse for the APF inverter.  $i_{Ca}^*$  signal is sent to HCC in order to generate proper switching pulses for the APF power inverter.

### 2.3 Hysteresis current controller

Among many other current controller techniques to generate switching pulse [17], the HCC is the most extensively used for APF. This is because it is simple in design, fast response, easy to implement and possess unconditioned stability [18-20]. The principal operation of the HCC is to generate the switching pulse for VSI by comparing the real current (actual signal) and reference current (reference signal) within the hysteresis bands. The switching frequency of HCC depends on the charging current from the upper-band to lower-band; accordingly, the switching frequency will be varying.

The principal operation of the DHCC [21] is different from HCC. In terms of the switching, pulse is generated by comparing within the upper-band, lower-band and the reference current (reference signal) [22]. The switching of G1 and G2 pulses are generated for the changing of the actual signal within upper-band and reference signal, while G3 and G4 are generated for the changing of the actual signal within lower-band and reference signal. Therefore, the G1 and G4 will be switching ON off both switching pulses overlap and vice-versa for G2 and G3.

The principal operation of the THCC is similar to DHCC [23]. Only the difference is of switching pulse that is generated for G1 and G4 by comparing within the upper-band and 2<sup>nd</sup> upper-band [24], where G2 and G3 by comparing within the lower-band and 2<sup>nd</sup> lower-band [25].

### 2.4 Determination of DC-link capacitor for SAPF

The SAPF DC bus reference voltage, ( $V_{DCref}$ ) for single-phase and three-phase (three wires and four wires) system can be determined by using (10) and (11):

$$V_{DC,min} \geq \frac{V_S}{\sqrt{2}m} \quad (10)$$

$$V_{DC,max} \geq \frac{2\sqrt{2}V_S}{\sqrt{3}m} \quad (11)$$

Where

$V_S$  = Source voltage, 240 V for single-phase

$m$  = Amplitude modulation index (ratio of inverter DC-link voltage to system peak voltage)

The  $m$  is considered as 1 because the inverter DC-link voltage had the same amplitude with the system peak voltage. Therefore, by using (10) and (11), the calculated values of  $V_{DC,min}$  and  $V_{DC,max}$  will be used to calculate the  $C_{DC}$  by using the (12) for single-phase system.

$$\frac{1}{2}C_{DC} \left[ (V_{DC,max})^2 - (V_{DC,min})^2 \right] = V_S(aI) \frac{T}{2} \quad (12)$$

Where

$a$  = Overloading factor

$I$  = Phase current supplied by the source to the load

$T$  = Time period of the system voltage (0.02 s)

The  $a$  is selected from its range of 120-180 % of steady-state current during the transient condition. It is selected with a value of 1.2 to 1.8. After obtaining the  $C_{DC}$  values, the selection of a capacitor must be closer and higher than the calculated value. For the SAPF design for 5 Amps current rating, the calculated  $C_{DC}$  values are in a range of 220  $\mu$ F to 330  $\mu$ F. In this paper, the chosen  $C_{DC}$  value is 330  $\mu$ F at 180 % overloading factor.

### 2.5 Determination of coupling inductance for SAPF

The selection of suitable series inductance values is crucial for the APF design, because it will affect the filtering ability and reducing the ripple for the compensated current [19]. In this paper, the inductance value is calculated based on the error analysis from the current ripple ( $I_r$ ).  $I_r$  is defined as the difference

between the compensate current and the reference current in pulse width modulation (PWM). For determining the maximum inductance value, firstly, we needed to find out the maximum current ripple ( $\Delta I_r$ ) and  $f_{sw}$ . These two values can be obtained from the  $I_r$  and  $T_s$  of the modulation signal with the current reference signal as shown in Figure 3.

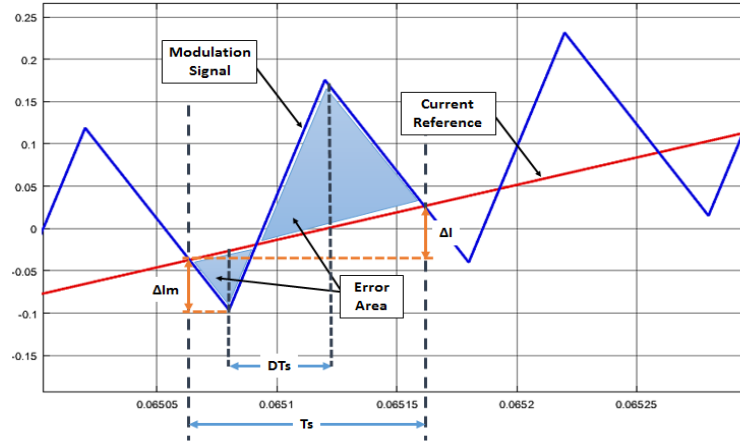


Figure 3. Current ripple of the modulation signal and current reference

From Figure 3, the collected value for  $\Delta I_m$  and  $\Delta I$  will be used to calculate the  $\Delta I_r$  value with (13):

$$I_r = \Delta I_m + \frac{(1-D)}{2} * \Delta I \tag{13}$$

After obtaining the  $\Delta I_r$  values, the  $L_{APF}$  values can be selected from the calculated range of suitable inductance with (14):

$$\frac{V_S - V_{DC,min}}{\omega * I_{max}} \leq L \leq \frac{V_{DC,max} - V_S}{4\Delta I_r * f_{sw}} \tag{14}$$

Where

$$\omega = 2\pi f_s$$

$I_{max}$  = Maximum current

$\Delta I_r$  = Maximum current ripple

$f_{sw}$  = Switching frequency, 10 kHz

For 5 Amps current rating single-phase SAPF, the calculated minimum inductance value is 40 mH and the maximum inductance is 59.48 mH (approximately to 60 mH). In order to find out the suitable inductance value for those SAPF with different switching devices, the calculated inductance values from 40 mH to 60 mH are tested with the non-linear loads along with 330  $\mu$ F capacitance. Table 1 shows the value of inductance which gives less THD for the non-linear loads with different switching devices VSI with HCC, DHCC and THCC. The selective values of inductance are based on the average inductance value. Therefore, simulation results of IGBT, MOSFET and Hybrid VSI based on 45 mH are as shown in Table 1.

Table 1. The less THD inductance value for different VSI

| Load              | Inductance value, mH |       |       |        |       |       |        |       |       |
|-------------------|----------------------|-------|-------|--------|-------|-------|--------|-------|-------|
|                   | IGBT                 |       |       | MOSFET |       |       | Hybrid |       |       |
|                   | HCC                  | DHCC  | THCC  | HCC    | DHCC  | THCC  | HCC    | DHCC  | THCC  |
| L1                | 50                   | 45    | 40    | 50     | 40    | 45    | 50     | 40    | 40    |
| L2                | 55                   | 40    | 40    | 50     | 40    | 45    | 50     | 45    | 45    |
| L3                | 50                   | 45    | 45    | 45     | 40    | 40    | 55     | 45    | 40    |
| L4                | 40                   | 40    | 40    | 50     | 45    | 40    | 50     | 45    | 45    |
| Average $L_{APF}$ | 48.75                | 42.25 | 41.25 | 48.75  | 41.25 | 42.25 | 51.25  | 43.75 | 42.25 |

### 3 RESULTS AND DISCUSSION

The supply voltage is 240  $V_{RMS}$  (340  $V_P$  and 680  $V_{pp}$ ). Therefore, it is expected that the  $V_{DC}$  value will increase if the load current increases. The  $V_{DC}$  will be swinging with a maximum voltage of 680  $V_{DC,PP}$  and 480  $V_{DC,RMS}$  values depending on the connected loads. Therefore, the selection of DC-bus reference voltage ( $V_{DC,ref}$ ) must be between the range of 340 V and 480 V. For this 390 $V_{DC,ref}$  value is selected for this paper. Figure 4 shows the simulation results of source current THD before and after connecting the designed SAPF with different VSI (IGBT, MOSFET and Hybrid).

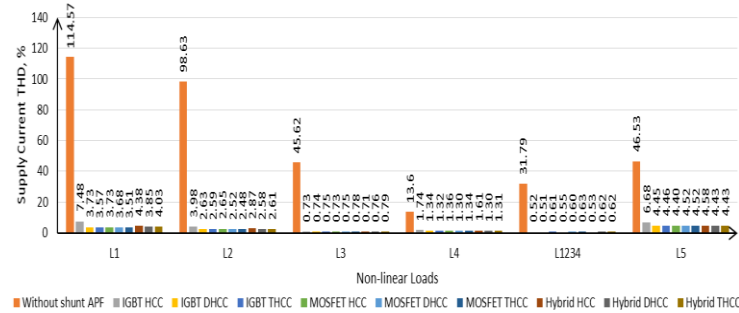


Figure 4. Source current THD before and after SAPF

Figure 5 shows the source current THD with the harmonic limit of IEEE-519 standard (%THD  $\leq$  5 %). From this, we can observe that the designed SAPF with HCC is working well for 3.73% to 0.52%, but with the excess harmonic limit of L5 as estimated. This is due to the L5 had a higher current rating. With HCC only the  $VSI_{IGBT}$  possess higher current THD for L1, L2 and L5, as expected, since IGBT produces higher compensate harmonics than MOSFET. The  $VSI_{MOSFET}$  and  $VSI_{HYBRID}$  had similar performance with HCC, DHCC and THCC as estimated. The VSI of MOSFET overall gives reasonable harmonic compensation along with HCC, DHCC and THCC compared to VSI of IGBT VSI. The VSI for the Hybrid DHCC and THCC do not show the significant improvement in current THD for 3.73% to 0.56%, but it is able to reduce the current THD below the standard limit for 4.43%. This proves the concept of a theory that the combination of IGBT and MOSFET (Hybrid VSI) is able to give better harmonic compensation for low current rating applications.

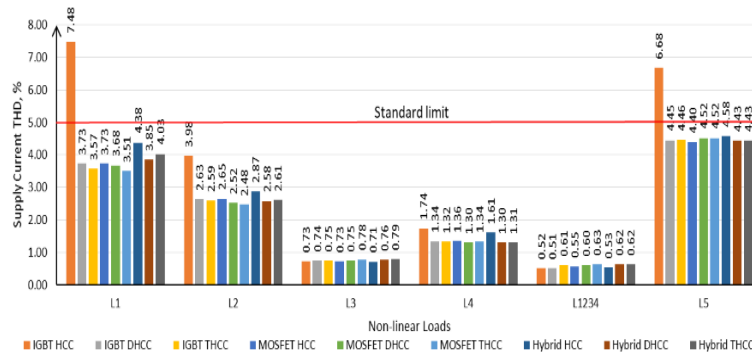


Figure 5. Source current THD after SAPF with the standard limit

Figure 6 shows the collected average switching frequency for HCC, DHCC and THCC. Table 2 shows the reduction of switching frequency of DHCC and THCC over HCC. From the collected results, we can see that the DHCC and THCC reduce the switching frequency significantly for L1 to L4 and L5. For L1234 it is less significant due to the standard limit. For this load the SAPF needs to compensate both even and triple-harmonic. The switching frequency of DHCC and THCC can reduce more, if the setting for the hysteresis band is more significant, as a result of  $THD_1$  increasing. This is due to lower the switching frequency, the compensate current becomes less than the real current signal and causes the  $THD_1$  to increase.

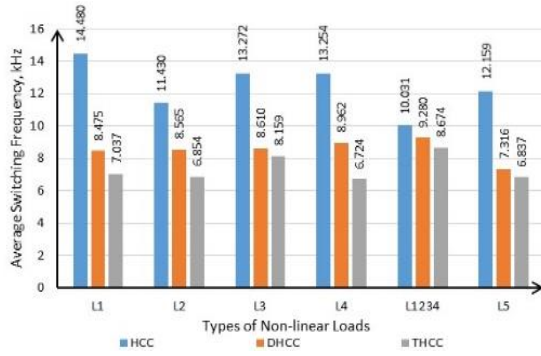


Table 2. Reduction of switching frequency in DHCC and THCC over HCC

| Load           | Reduction of SW,%<br>DHCC | THCC   |
|----------------|---------------------------|--------|
| L1             | 41.471                    | 51.402 |
| L2             | 25.066                    | 40.035 |
| L3             | 35.127                    | 38.525 |
| L4             | 32.383                    | 49.268 |
| L1, L2, L3, L4 | 7.487                     | 13.528 |
| L5             | 39.831                    | 43.770 |
| Average        | 36.273                    | 47.306 |

Figure 6. Collected average switching frequency for HCC, DHCC and THCC

Since, the HCC had variable switching frequency, the collected average frequency shown in Figure 6 is used to calculate the power loss of the respectively simulated VSI which is shown in Figure 7. For L1 to L1234, low current, the HCC produce high switching frequency so the  $VSI_{IGBT}$  had more power losses due to switching loss. However, when current increases,  $VSI_{MOSFET}$  had high conduction loss and causing higher power loss and increasing the  $VSI_{IGBT}$  at L5. While the  $VSI_{HYBRID}$  show less significant reduction in power loss compared to  $VSI_{IGBT}$  and  $VSI_{HYBRID}$ . While the higher load current of L5 it shows less power loss than  $VSI_{MOSFET}$  and  $VSI_{IGBT}$ . However, applying DHCC and THCC for  $VSI_{IGBT}$ , significantly reduce the power loss for  $VSI_{IGBT}$ . This is because the primary power loss in IGBT is switching loss.  $VSI_{HYBRID}$  DHCC and  $VSI_{HYBRID}$  THCC t show less power loss compared to  $VSI_{MOSFET}$  DHCC and  $VSI_{MOSFET}$  THCC hen the current increases for L5. This proves the theoretical assumption that the  $VSI_{HYBRID}$  will be able to serve the advantages of both IGBT and MOSFET by providing a low power loss of VSI and better harmonic compensation for low switching frequency at higher current rating applications.

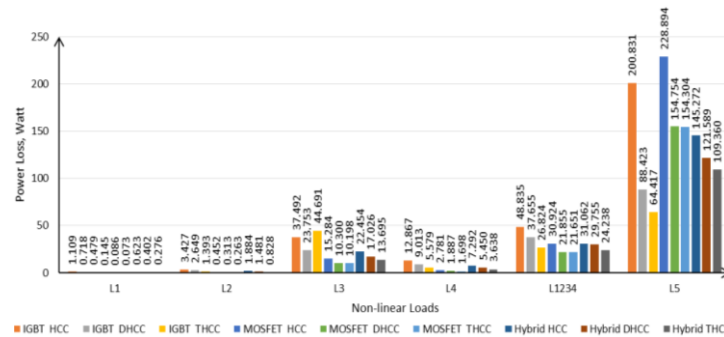


Figure 7. Calculated power loss in VSI with non-linear loads

#### 4 CONCLUSION

In this paper, the performance of SAPF based on PQ theory with different types of  $VSI_{HCC}$ ,  $VSI_{DHCC}$  and  $VSI_{THCC}$  current controllers are investigated. Simulation results show that at the proper selective of coupling inductance, the switching devices will be able to improve the capability of harmonic compensation. From the simulation results, it also can be concluded that the  $VSI_{MOSFET}$  and  $VSI_{HYBRID}$  give similar and better harmonic compensation compared to  $VSI_{IGBT}$  when the current is increased. However, the performance of  $VSI_{IGBT}$  is improved along with DHCC and THCC, as well as provided fewer power losses compared to others. Therefore, by using DHCC and THCC for VSI, it not only just reduces the power loss, but also improve the SAPF capability for using the L5 that has a higher current rating than the designed current rating (5 Amps). The  $THD_{iDHCC}$ ,  $THD_{iTHCC}$  or all types of switching devices of voltage inverter are below the IEEE-519 standard harmonic limit. The DHCC and THCC are able to reduce the switching frequency at an average of 35 % and 45 % respectively over the HCC. So, the simulation' results proved the usage of DHCC and THCC and are able to improve the SAPF performance for the rating of 3 times

higher current loads. This can conclude that, the  $VSI_{IGBT}$  THCC is the best combination of VSI, because it provides the least power loss and proper harmonic compensation (THD<sub>i</sub> less than 5 %). In this paper the power loss of SAPF is estimated with the collected average switching frequency. This is because of the fixed PI voltage controller which is used for regulating the DC-link voltage

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