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Multi Carrier based Multilevel Inverter with Minimal Harmonic Distortion

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ABSTRACT

This paper presents performance features of Asymmetric Cascaded Multilevel inverter. Multilevel inverters are commonly modulated by using multicarrier pulse width modulation (MCPWM) techniques such as phase-shifted multicarrier modulation and level-shifted multicarrier modulation. Amongst these, level-shifted multicarrier modulation technique produces the best harmonic performance. This work studies about multilevel inverter with unequal DC sources using level shifting MCPWM technique. The Performances indices like Total Harmonic Distortion (THD), number of switches and DC Sources are considered. A procedure to achieve an appropriate level shifting is also presented is this paper.

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1. INTRODUCTION

The multilevel inverter has introduced the solution to increase the converter output voltage above the voltage limits of classical semiconductors. It finds its application mainly in industries such as AC power supplies, static VAR compensators, drive systems, etc. A new hybrid asymmetric multilevel inverter was introduced where 27 levels is obtained with minimum number of switches. This achieves a better sinusoidal output [1]. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [2]. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero [3]. The multilevel inverters are basically classified into three topologies, they are as follows, the flying capacitor inverter, the diode clamped inverter and the cascaded H-bridge inverter. All the topologies have same property of reducing the harmonics [4]-[6]. Cascaded inverter has the disadvantage that it needs separate DC sources but the circuit layout is compact and voltage sharing problem is absent. Due to these advantages, the cascaded inverter bridge has been widely applied to such applications as HVDC, SVC, stabilizer, high power motor drive and so on [7], [8]. The various modulation strategies have been introduced for the cascaded multi level inverters inorder to reduce the harmonic contents [9]. Multilevel inverters with their topologies were introduced. Of all the topologies cascaded has many advantages when compared with diode clamped and capacitor clamped inverter [10] [11].

A further study on cascaded multilevel inverters was performed in order to highlight the advantage of cascaded multilevel inverter when compared with the other topologies and the switching characteristics sare analysed. The concept of sinusoidal PWM modulation was introduced in an attempt to reduce the

harmonic contents at the output voltage. Level shifted modulation technique gives better result compared with the phase shifted. Level shifting is done to reduce the harmonics at the output voltage [12]-[14]. This paper will investigate a control technique applied to the Hybrid asymmetric cascaded multi-level inverter in order to ensure an efficient voltage utilization and better harmonic spectrum. Level shifting is a well-established emerging modulation and control techniques has been designed and discussed. The level shifting methods have been introduced and results were presented.

2. HYBRID MULTILEVEL INVERTER

The structure introduced in this work is an Asymmetric cascaded multilevel inverter, which uses unequal DC Sources. The general function of this multilevel inverter is the same as that of the other two inverters. The multilevel inverter using Asymmetric cascaded-inverter provides a large number of output voltage levels without increasing the number of full bridge units. This configuration provides higher voltage at higher modulation frequency due to which the topology can be employed for high power applications. Due to the reduction in the number of DC Sources employed, the structure becomes more reliable and the output voltage has higher resolution due to increased number of steps. This configuration recently becomes very popular in AC power supply and adjustable speed drive applications. This inverter can avoid extra clamping diodes or voltage balancing capacitors [4]. An Asymmetric cascaded H-bridge inverter circuit is shown in Figure 1.

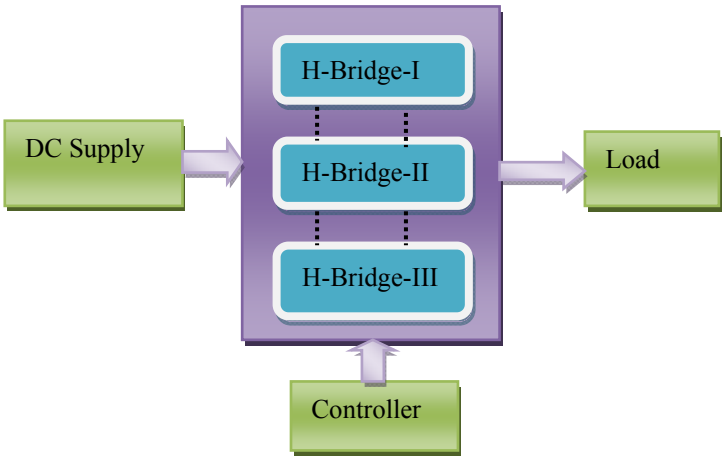


Figure 1. Structure of ternary voltage cascaded multilevel inverter

Table 1. Switching state for positive voltage

V	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
1	1	1	0	0	0	1	0	1	0	1	0	1
2	0	0	1	1	1	1	0	0	0	1	0	1
3	0	1	0	1	1	1	0	0	0	1	0	1
4	1	1	0	0	1	1	0	0	0	1	0	1
5	0	0	1	1	0	0	1	1	1	1	0	0
6	0	1	0	1	0	0	1	1	1	1	0	0
7	1	1	0	0	0	0	1	1	1	1	0	0
8	0	0	1	1	0	1	0	1	1	1	0	0
9	0	1	0	1	0	1	0	1	1	1	0	0
10	1	1	0	0	0	1	0	1	1	1	0	0
11	0	0	1	1	1	1	0	0	1	1	0	0
12	0	1	0	1	1	1	0	0	1	1	0	0
13	1	1	0	0	1	1	0	0	1	1	0	0

In this proposed model trinary DC voltages progressions of unequal DC sources of ACMLI are used. This is most popular of unequal voltage progression with amplitude of DC voltage having ratio 1:3:9:27; 81....3N and the maximum output voltage reach to ((3N-1)/2) V_{dc}. ACHB consist of 3-bridges is used to generate 27 level output for the DC Sources of 9:3:1 ratio. The output waveform 27 levels as ±13Vdc …. ±1Vdc and zero. By different combinations of the 12 switches, S1-S12, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero. Let the output of H bridge-1 is denoted as V_1 (t), the output of H bridge-2 is denoted as V_2 (t) and H bridge-3 is denoted as V_3(t). Hence the output voltage is given by

$$V(t) = V_1(t) + V_2(t) + V_3(t) \quad (1)$$

Switching states are developed for positive, negative and zero voltages as per the patterns given in the switching Table 1. The generated gate pulses are given to each switch in accordance with the developed pattern and thus the output is obtained.

3. MULTICARRIER BASED MODULATION METHODS

Pulse Width Modulation refers to a method of carrying information on a train of pulses, the information is encoded in the width of each pulse. This technique helps in maintaining a constant voltage. A modulation strategy for multilevel inverters is given in Figure 2. In the carrier-based multilevel modulation, each level in a phase requires a carrier of its own. Carrier- based modulation schemes are mainly divided into two categories: level-shifted (LSPWM) and phase-shifted (PSPWM) methods. Both of these have several variations, which differ by the allocation of module carriers with respect to each other.

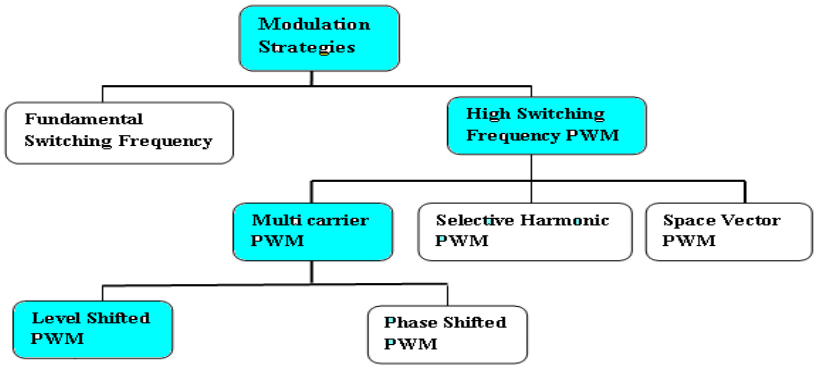


Figure 2. Modulation strategies for multilevel inverters

In all level-shifted PWM methods, the carriers of the modules have a frequency of f car = 1/Tsw where the frequency of the carrier signal is inversely proportional to the switching period of the device (The range of the f car is selected between 10 kHz to 100kHz). The reference voltage, on the other hand, can have values of the range −MVdc and MVdc. To cover the whole voltage range, the carriers are the triangular waves with same phase and peak to peak amplitude and arranged vertically, so that the carrier of the first module covers the range from zero to Vdc, while the second covers the range from Vdc to 2Vdc. The last module covers the voltage from (M−1)Vdc to MVdc.This method are generally used in CMLI as it gives reduced THD. Therefore, an inverter with M- modules in series is usually referred to as an n-level inverter and the number of levels can be calculated as given in Equation (2).

$$n = 2M + 1 \quad (2)$$

There are three kinds of level shifted modulation techniques namely; Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD), Phase Disposition (PD). In the phase opposition disposition (POD) the carriers above the reference point, are out of phase with those below zero, by 180 degree. In the alternative phase opposition disposition (APOD), the carriers of adjacent bands are phase shifted by 180 degree. In the phase disposition (PD), all the carriers are in phase across all the bands. This gives rise to the lowest harmonic in the higher modulation indices, when compared to the other disposition

methods. The level shifted multicarrier modulation offers better harmonic attenuation, but also offers an unequal device condition.

4. RESULT AND DISCUSSIONS

The feasibility of the proposed PWM strategy has been investigated and verified through simulation results, for both multilevel inverter and multi carrier PWM inverter, for a twenty seven level cascaded asymmetric H-Bridge inverter. The proposed technique for a twenty seven levels inverter with asymmetric DC sources involves the usage of only three DC cells. The voltages are given in the ratio of 9:3:1 with which a twenty seven level can be achieved with only three DC sources. The simulink model for a twenty seven level MLI is shown in Figure 3 they are created with a separate subsystem. The pulses are generated with the developed pattern and given to the corresponding switches via the subsystems. The 27 level output voltage is shown in Figure 4(a). Higher the level, the harmonics are reduced to greater extent. To determine the harmonics in the proposed circuit, the FFT analysis is performed which is shown in Figure 4(b).

This is the logical extension of the sine triangle PWM multilevel inverter, in which n-1 carriers are needed for an n-level inverter. The preferred type is Phase disposition. The carriers are arranged in vertical shifts in continuous bands defined by the levels of the inverter. Each carrier has the same frequency and amplitude. An n-level inverter using level shifted multicarrier modulation scheme requires (n-1) triangular carriers, all having same frequency and peak to peak amplitude, hence for 27-level inverter, 26 carriers are used. Modulation is generally performed in any circuit to reduce the harmonic content at the output voltage. The harmonic content after modulation is analysed by the FFT spectrum shown in Figure 5(a), and 5(b) respectively. It is clear from the FFT analysis that the harmonics are reduced to a greater extent after modulation. The variations of the harmonic content present at the output voltage before and after modulation are clearly seen from the FFT spectrum.

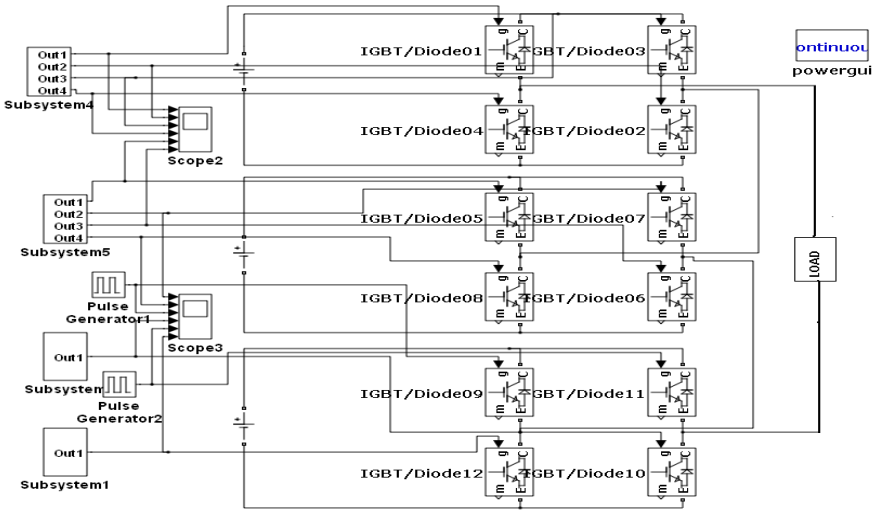
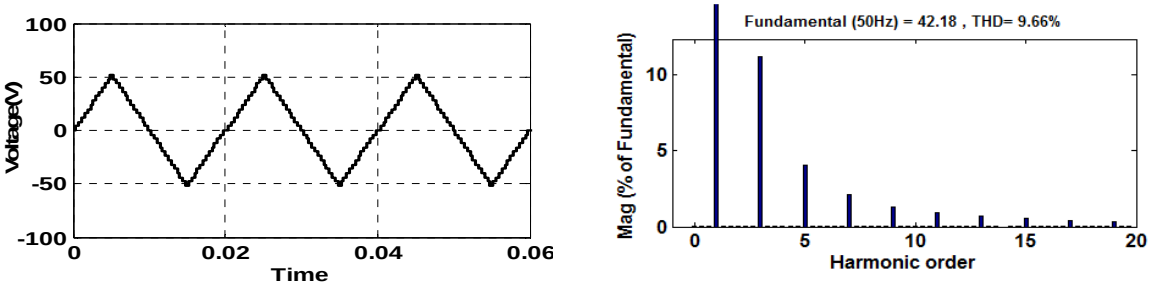


Figure 3. Simulink model of Asymmetric multicarrier PWM inverter

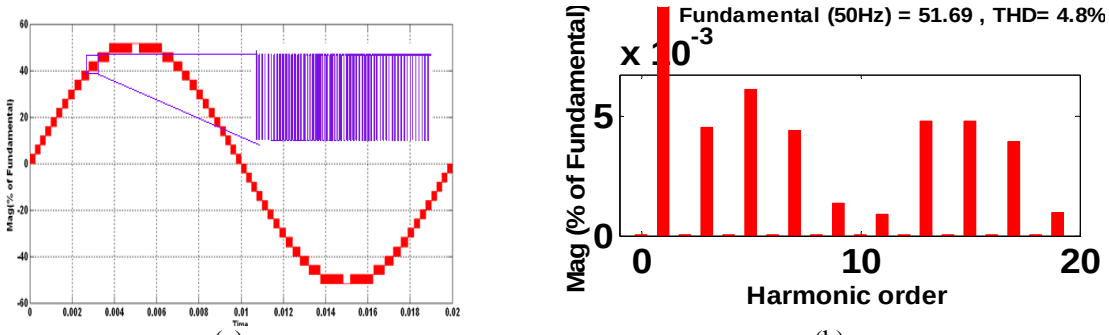
With the same circuit the other modulations are also performed. Variations are only with the multicarrier that has been generated. Only difference is with the carriers that has been generated inside the subsystems for both positive and negative cycles. The main circuit model remains the same for the other two modulations. Also their FFT analysis is performed to analyse the harmonics. A comparative study has been made to demonstrate the superiority of the Asymmetric cascaded multi level inverter over symmetric MLI and presented in Table 2. From the table it is observed that for the same number of bridges, switches, asymmetric MLI provides more number of levels. From the FFT analysis it is observed that the total harmonic distortion content at output waveform for 27 level inverter is found to be quite high and it does not meet to international IEEE standard. So to reduce the THD content further, multicarrier PWM technique is introduced Aymmetric Cascaded MLI.

It is found that THD is considerably reduced after modulation is being performed. From the previous work it is known that the PD technique produces fewer harmonic on a line-to-line basis compared to the other two techniques because it puts harmonic energy directly into a common mode carrier component which cancels across the line-to-line outputs [2]. THD content is reduced by applying modulation scheme. From the comparison made between different modulation schemes, PD Technique proved to be the best modulation techniques compared to the other modulation techniques.



(a) (b)

Figure 4. (a) Simulated output waveforms of Asymmetric Multilevel inverter
(b) Harmonics Spectrum of output voltage waveform



(a) (b)

Figure 5. (a) Output voltage of PD modulation; (b) Harmonic spectrum of Output voltage (PD)

Table 2. Comparison of Asymmetric Multilevel inverter with and without modulation

Parameters	Symmetric MLI		Asymmetric MLI	
	Without Modulation	Level Shifted Modulation	Without Modulation	Level Shifted Modulation
Number of switches	12	12	12	12
Number of DC Sources	3	3	3	3
Fundamental voltage	42.47	50.12	44.18	51.69
h3	9.24	6.41	11.18	0.17
h5	2.04	1.03	4.07	0.24
h7	3.79	1.60	2.12	0.23
h9	3.83	0.17	1.31	0.83
Distortion factor(DF_1)	0.122432	0.012843	0.0596	0.012835
Distortion factor(DF_2)	0.023249	0.018015	0.0122	0.00137
THD%	25.09	18.89	9.66	4.8

5. CONCLUSION

Optimal switching strategy of multicarrier for Hybrid Asymmetric Multi Level Inverter has been presented. Simulink models for various level shifting methods like PD and APOD are presented. The behaviour of hybrid multi level inverter is presented with and without implementing Multicarrier strategy. Asymmetric MLI Topology uses reduced number of DC sources thus decreasing the complexity and the cost of the circuit. Moreover, this approach enables to obtain a twenty seven-level conversion with only three dc bus levels. This reduces the cost and offers the more number of levels at the output with a least number of

primary devices and DC voltage sources. The results for both of the techniques are then compared against various performance indices. From the comparison, it is observed the THD obtained with MCPWM Inverter is lesser than the MLI. By increasing the number of steps, waveform approaches the desired sinusoidal shape and THD is reduced to IEEE standard. Proposed work can be extended to three phase and the same can be realised in hardware to drive high power motors such as PMBLDC motors and so on.

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