

## Comparison of Multilevel Inverters for the Reduction of Common Mode Voltage

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### ABSTRACT

This paper presents a comparison between NPC (neutral point clamped) and H-cascaded multilevel inverters by considering the increase or decrease of harmonics in the output line to line voltages, phase voltages and common mode voltage. Multilevel voltage source converters are getting increased importance for applications in the medium and high voltage range. A conventional two-level PWM (pulse width modulated) inverter generates high frequency common mode voltage with high dv/dt. In the same way, commonly used multilevel inverter modulation schemes generate common mode voltage. Common mode voltage may cause motor shaft voltages, bearing currents and EMI (electromagnetic interference). Common mode voltage depends not only on switching method but also on earth mass. The use of earth mass on a proper place in the circuit can reduce the common mode voltage. Sinusoidal (sine-triangle) PWM scheme is being used for this purpose and simulation results are being presented in this paper by using software "Simplorer" and "Post Processor Day".

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## 1. INTRODUCTION

Due to increasing demand of energy, multilevel converters are being getting importance because of improved harmonics and low Electromagnetic Interference (EMI). Many modulation schemes have been used up to this time for multilevel inverters. Carrier based modulation strategy is being used to reduced harmonics in multilevel converters. Several types of multilevel converters have been investigated for these new applications [1-7]. The basic requirements for this application field are high voltage and high power. Besides this, many other aspects, regarding to the industrial implementation of these converters, have to be taken into consideration. To overcome the shortcomings in solid state switching device ratings, multilevel converters have been developed, so that they can be applied to high voltage electrical systems.

The neutral point clamped inverter (also called diode clamped inverter) shown in figure 1 uses a single dc bus that is subdivided into a number of voltage levels by a series string of capacitors [8]. Similarly a H-cascaded inverter uses a single dc bus but that is not subdivided. A matrix of semiconductor switches and diodes allows each phase leg output to be switched to any of these voltage levels. Pulswidth modulation (PWM) sine triangle has been used for this work.

At supply voltages, bearing currents may flow in a closed loop comprising the shaft, both end-shields and the housing. These circulating currents are caused by magnetic asymmetries of the stator yoke, which result in a ring flux in the yoke inducing the so-called shaft voltage in the loop. Up to a certain value of the shaft voltage the circulating current is zero; however, at higher shaft voltages the circulating currents destroy the bearing within a short period of time. In many cases the shaft voltage can be limited to uncritical values by optimization of the yoke geometry; otherwise the insulation of one bearing is a common measure

of protection. Novel effects occur at supply by modern voltage source converters (VSC), caused by capacitive coupled bearing voltages, which initiate the so-called EDM-currents (Electric Discharge Machining) through one motor bearing, and by shaft voltages of high frequency. This effects result from the common mode voltage of the inverter which represents a zero sequence component of the voltages and which is inherent to all control schemes of PWM inverters.

## 2. STRUCTURE AND OPERATION OF MULTILEVEL INVERTERS

A three phase three level neutral point clamped and H-cascaded inverter are shown in figure 1 and 2. Each of three phases of the inverter shares a common dc bus voltage, which has been subdivided into three levels.

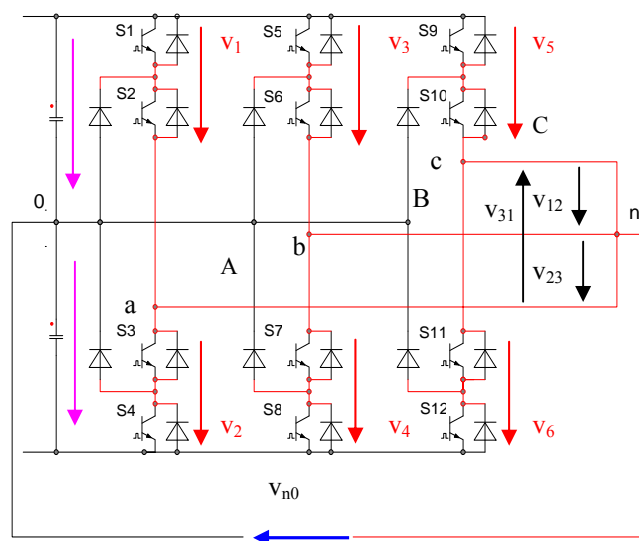


Figure 1. Structure of a three level diode clamped inverter

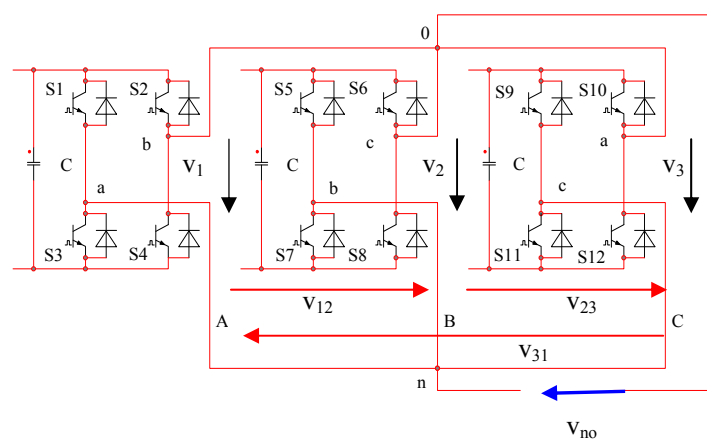


Figure 2. Structure of a three level H-cascaded inverter

The voltage across each capacitor is  $V_{dc}/2$  and the voltage stress across each switching device is limited to  $V_{dc}/2$  through the clamping diodes in figure 1 and  $V_{dc}$  for H-cascaded in figure 2. Each phase has two complimentary switch pairs such that turning on one of the switches of the pair requires that the other complimentary switch be turned off. The complimentary switching pairs for phase legs are (S1, S3) and (S2, S4), for (S5, S7) and (S6, S8) and (S9, S11) and (S10, S12).

A cascaded multilevel inverter (figure 2) consists of H-bridge (single-phase full bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate

dc sources. Each inverter level of H-cascaded inverter can generate three different output phase voltages,  $+V_{dc}$ ,  $0$  and  $-V_{dc}$  by connecting the dc sources to the ac output side by different combination of four switches S1, S2, S3 and S4, where as NPC inverter generates five output phase voltages  $+2V_{dc}$ ,  $+V_{dc}$ ,  $0$ ,  $-2V_{dc}$  and  $-V_{dc}$  (figure 4). The phase voltage depends on the number of levels. With enough levels, using this fundamental switching technique results in an output voltage of the inverter that is almost sinusoidal. Inversely the line to line voltage of H-cascaded inverter shows 5 voltages  $+2V_{dc}$ ,  $+V_{dc}$ ,  $0$ ,  $-2V_{dc}$  and  $-V_{dc}$  and NPC inverter 3 voltages  $+V_{dc}$ ,  $0$  and  $-V_{dc}$  respectively (figure 3). Figures 5 and 6 show the spectrum of output line to line and phase voltages.

### 3. DESCRIPTION

Typically, two kinds of bearing currents are caused by the bearing voltage which pass only one bearing of the motor and flow back to the converter. The so-called du/dt-currents through the capacitor of the bearing are less than maximal several hundred mA and therefore they cannot destroy the bearings. By contrast, the EDM-currents, stochastically occurring break downs of the grease film at high peak values of the bearing voltage, are of great practical importance. The endangering factors are the peak values of the EDM-currents and its repetition rate. The repetition rate grows with the switching frequency. The common mode voltage causes common mode currents. It depends on the kind of grounding system whether these zero sequence components of the currents penetrate the active parts of the motor. Statistics of bearing faults show that many bearing deficiencies at converter supply are caused by poor grounding for frequencies in the kHz range. The common mode currents penetrating the stator winding don't cause a linear voltage drop along the length of the winding conductors, because they flow partly through the capacitor between winding and core. Consequently the currents in the two leads of each turn are not yet identical. The impulse shaped shaft voltage obviously acts as initiator for the circulating currents, the emf of which is the shaft voltage of basic frequency. This relationship was unknown up to now [9]. The power circuit of a three phase and three level inverter is shown in figure 2. Assuming that of the two power switches in each leg of the inverter one and only one is always on, that is, by neglecting the time intervals when both the switches are off (blanking time), three switching variable phases a, b, and c can be assigned to the inverter. It is easy to show that the instantaneous line to line output voltages, as described in equ. (1-2),  $v_{12}$ ,  $v_{23}$  and  $v_{31}$  are given by:

NPC-inverter:

$$\begin{bmatrix} v_{12} \\ v_{23} \\ v_{31} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (1)$$

H-cascaded inverter:

$$\begin{bmatrix} v_{12} \\ v_{23} \\ v_{31} \end{bmatrix} = V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & - & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2)$$

NPC-inverter:

$$\begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (3)$$

H-cascaded inverter:

$$\begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (4)$$

In equations (1-4) a, b, and c are the phase legs.

The equations (1-4) give the line to line ( $v_{12}$ ,  $v_{23}$ ,  $v_{31}$ ) and phase ( $v_{An}$ ,  $v_{Bn}$ ,  $v_{Cn}$ ) voltages of the neutral point clamped and H-cascaded inverter respectively, while the equations (5-6) give the common mode voltages ( $v_{cm}$ ) for NPC and (7-14) give for H-cascaded inverter derived from figure 1 and 2. The equations (5-6)

have been derived for common mode voltage ( $v_{cm} = v_{n0}$ ) for a two level and three phase inverter in [10-11] and have been interpreted here for NPC inverter. For H-cascaded inverter the equations (7-14) have been derived from figure 2 by using Kirchoff's law of voltages ( $\Sigma KLV = 0$ ).

NPC-inverter:

$$v_{n0} = \frac{V_{dc}}{6}(s_a + s_b + s_c) \quad (5)$$

$$v_{n0} = \frac{v_1(t) + v_3(t) + v_5(t)}{3} + \frac{V_{dc}}{2} \quad (6a)$$

$$v_{n0} = \frac{v_2(t) + v_4(t) + v_6(t)}{3} - \frac{V_{dc}}{2} \quad (6b)$$

H-cascaded inverter:

$$v_{cm} = v_{no} = v_1 + v_{An} \quad (7)$$

$$v_{cm} = v_{no} = v_2 + v_{Bn} \quad (8)$$

$$v_{cm} = v_{no} = v_3 + v_{Cn} \quad (9)$$

where as in equations (7-9)  $v_1$ ,  $v_2$  and  $v_3$  are given as:

$$v_1 = v_a - v_b \quad (10)$$

$$v_2 = v_b - v_c \quad (11)$$

$$v_3 = v_c - v_a \quad (12)$$

Putting the values of  $v_1$ ,  $v_2$  and  $v_3$  from equations (10-12) in equations (7-9) and adding give the value of common mode voltage:

$$3v_{cm} = v_a - v_b + v_b - v_c + v_c - v_a + (v_{An} + v_{Bn} + v_{Cn}) \quad (13)$$

As the last is symmetric in figure 2, therefore the sum of the output phase voltages ( $v_{An} + v_{Bn} + v_{Cn} = 0$ ) is zero and therefore the common mode voltage in equation (13) is zero and gives the equation (14) as:

$$v_{cm} = 0 \quad (14)$$

From equation (5), it is to see that the maximum amplitude of common mode voltage for NPC inverter will be  $V_{dc}/2$  if  $S_a = S_b = S_c = 1$  and will be  $-V_{dc}/2$  if  $S_a = S_b = S_c = -1$ , where  $S_a$ ,  $S_b$  and  $S_c$  are the switching functions of phase legs a, b and c. Similarly, the common mode voltage in equation (6) will be  $\pm V_{dc}/2$ , as  $v_1(t) + v_2(t) + v_3(t) = 0$ , and can be verified from figure 7a. For H-cascaded inverter the common mode voltage will be zero according to equation (14) and shown in figure 7b.

#### 4. SIMULATION RESULTS

For the circuits in figures 1 and 2, the dc bus voltage has been taken as 3.81kV. The figure 3 shows the output line to line voltage, which is equal to dc bus voltage for NPC and twice than that of dc bus voltage for H-cascaded inverter. It depends on the switching method of the switches. Figure 4 shows output phase voltage, which is  $2V_{dc}/3$  for NPC and  $V_{dc}$  for H-cascaded inverter according to the circuit shown in figure 1

and 2, where as figures 5 and 6 show the spectrum of the line to line and phase voltages. Figures 7 and 8 show the common mode voltage and its spectrum, which verify the equations (5-6) and (14). It will also be here mentioned that for circuits in figure 1 and 2, the basic and switching frequencies have been taken as 50Hz and 3kHz respectively. A filter was also used to reduce harmonics, but it showed no affect on the diagram ms, therefore the simulation results with a filter have not been shown here.

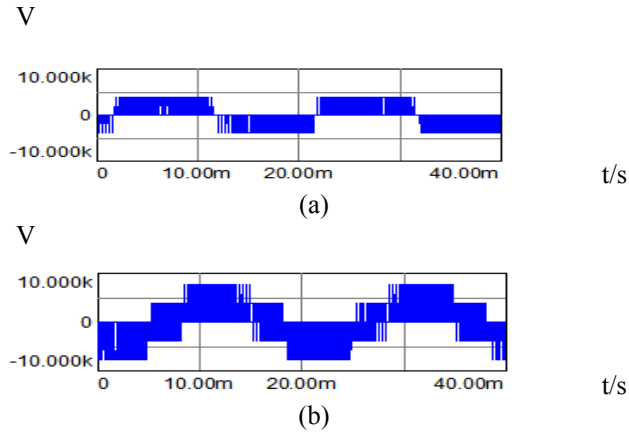


Figure 3. Line to line voltage (a) NPC (b) H-cascaded inverter

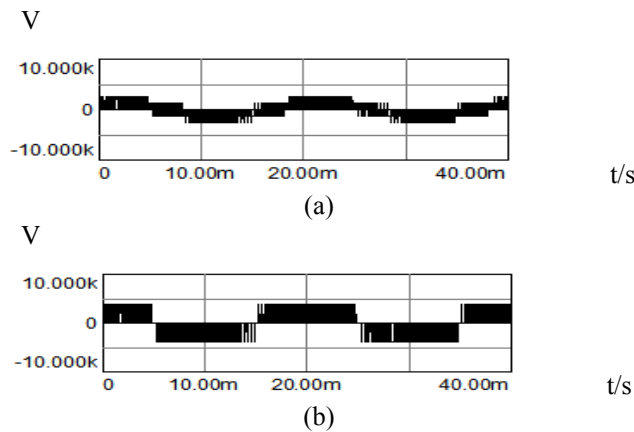


Figure 4. Phase voltage (a) NPC (b) H-cascaded inverter

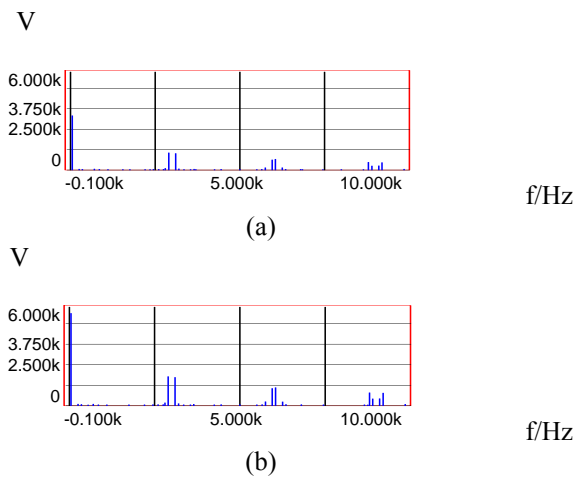


Figure 5. Spectrum of line to line voltage (a) NPC (b) H-cascaded inverter

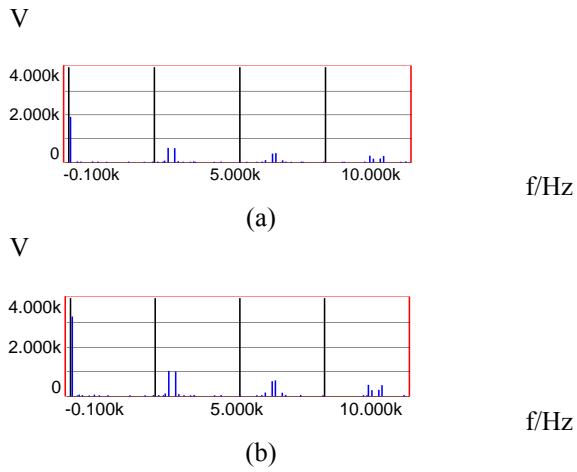


Figure 6. Spectrum of phase voltage (a) NPC (b) H-cascaded inverter

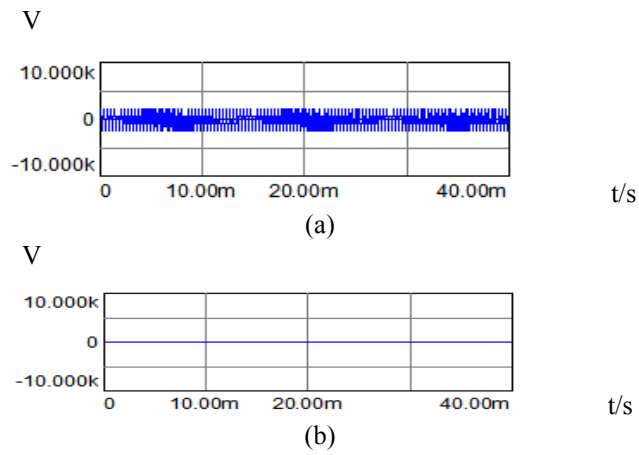


Figure 7. Common mode voltage (a) NPC (b) H-cascaded inverter

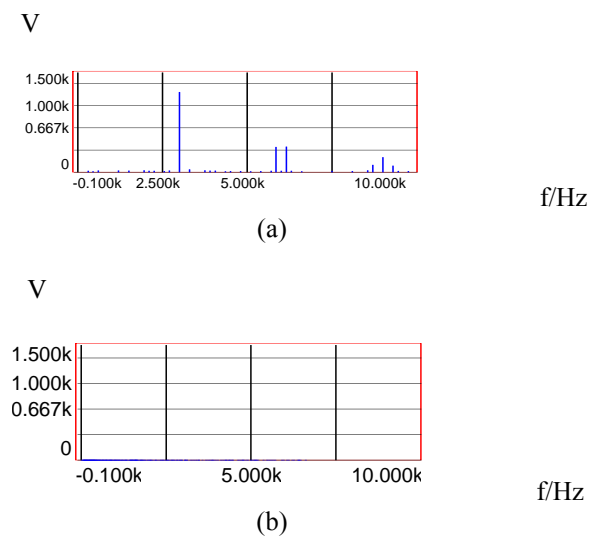


Figure 8. Spectrum of common mode voltage (a) NPC (b) H-cascaded inverter

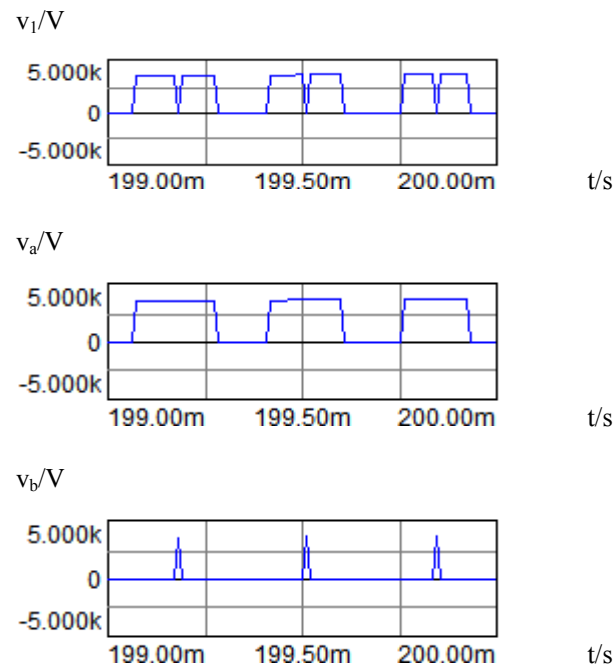


Figure 9. Voltages ( $v_1$ ,  $v_a$ ,  $v_b$ ) according to equation 10

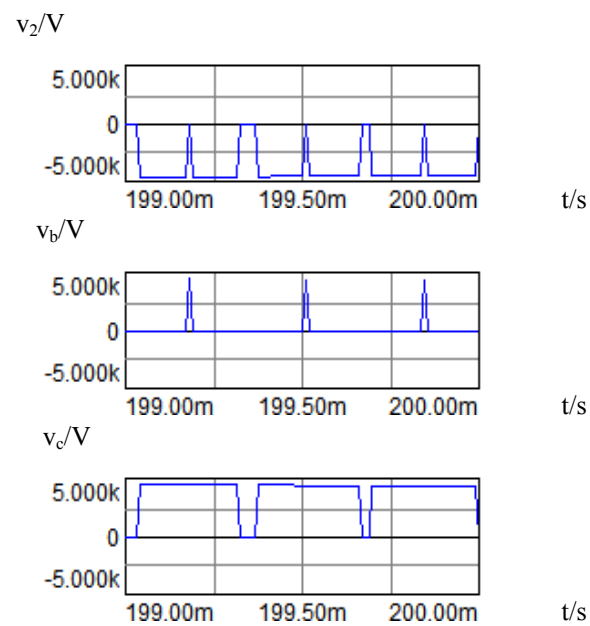


Figure 10. Voltages ( $v_2$ ,  $v_b$ ,  $v_c$ ) according to equation 11

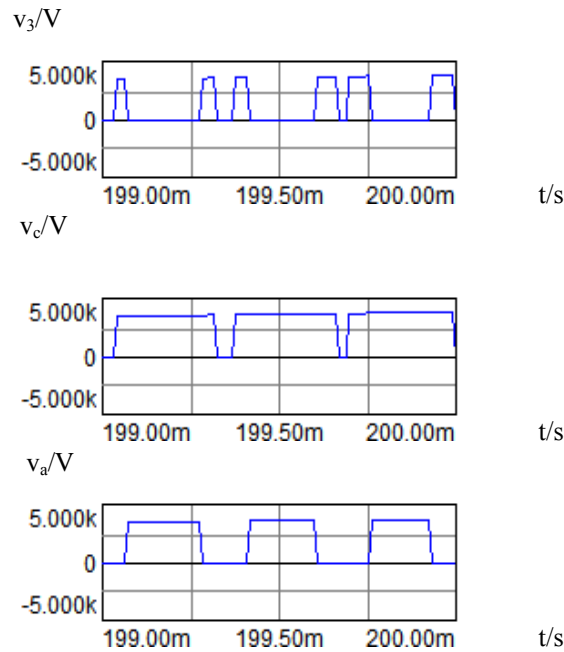


Figure 11. Voltages ( $v_3$ ,  $v_c$ ,  $v_a$ ) according to equation 12

## 5. CONCLUSION

From these simulation results it is to see that H-cascaded inverter is better than NPC inverter for the reduction of common mode voltage, which has been reduced to zero. Line to line output voltage for H-cascaded inverter is twice than that of NPC inverter. Output phase voltage of H-cascaded inverter is also greater than that of NPC inverter.

## ADVANTAGES AND DISADVANTAGES

Multilevel inverter have many advantages over a conventional two level inverter that uses a high switching frequency PWM. Multilevel inverters produce smaller common mode voltage, through which the stress in the bearings can be reduced. Multilevel inverter can operate at both fundamental and high switching frequency. These inverters can draw input current with low distortion. The output voltage of these inverters has low distortion and therefore EMC (electromagnetic compatibility) problems can be reduced, also due to reduction of  $dv/dt$  stress. Multilevel NPC and H-cascaded have the following advantages and disadvantages.

+ Advantage:      - Disadvantage:

### NPC inverter

- + For fundamental frequency switching is the efficiency high.
- + The capacitors can be pre charged as a group.
- + All the phases share a common dc bus, which minimises the requirements of the converter.
- + Circuit is not as costly as H-cascaded inverter.
- Topology of NPC inverter is difficult.
- Additional diodes are required

### H-cascaded inverter

- + Number of levels can be easily increased and also through that the output power.
- + The output line to line voltage is twice than the number of dc sources.
- + Topology is very easy.
- + No additional diodes are required as in NPC inverter.
- Separate dc sources are needed for each of the H-bridge.
- It is very expensive.



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