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Regeneration of ZVS converter with Resonant Inductor

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Abstract

This paper presents an analysis of the regeneration of zero-voltage-switching converter with resonant inductor, quasi-resonant converters, and full-bridge zero-voltage-switched PWM Converter. The design of a clamping circuit considering a saturable resonant inductor is presented and compared with the design of a clamping circuit with a linear resonant inductor. A diode model with reverse recovery is employed to simulate the effects.

Keywords: Converter, resonant inductor, PWM, ZVS, zero-voltage

1. Introduction

The zero-voltage-switching quasi-resonant converters (ZVS-QRCs) are appropriate to operate at switching frequencies of the several MHz, due to the reduced switching losses. However, their practical applications are limited because of the following limitations.

- High voltage stress on the Mosfet,
- Dissipative "mutation at light load,
- High frequency range to regulate the output voltage.

Those difficulties arise because the energy stored in a linear inductor is proportional to the square of the load current. The situation is different when the linear inductor is replaced by a saturable inductor.

The full-bridge zero-voltage-switched PWM converter (FBZVS- PWM) achieves ZVS by using the resonant inductor energy to discharge the output capacitance of the power switches, the load range under which ZVS is maintained is strongly dependent on the resonant inductance. For some applications which are sensitive to light load efficiency, a considerably large resonant inductor will be required to ensure ZVS at light load. Due to this large resonant inductor, the FB-ZVS-PWM converter operates with high circulating energy, which increases the conduction losses**,** and current and voltage ***stress*** of the switches In both converters, the linear resonant inductor interacts with the diode junction capacitances, causing severe parasitic oscillations, and increasing switching loss and switching noise. A simple technique to overcome the above-mentioned drawbacks of the ZVS-QRCs was presented and extended to FB-ZVS-PWM. It consists of replacing the linear resonant inductor by a saturable resonant inductor.

The operation of the ZVS-QRCs with a saturable inductor is fully described, and the operation of the FB-ZVSPWM with a saturable inductor is fully described.

The saturable inductor has been successfully applied to ZVS QRCs and to the FB-ZVS-PWM converter to improve their performance. It is shown in this paper that the employment of a saturable inductor *can* reduce parasitic oscillation between the diode junction capacitance and the resonant inductor. This parasitic oscillation is reduced, since the resonant inductor gets saturated, when the diode junction capacitance starts to resonant with it.

A complete analysis and design of a clamping circuit considering, a saturable resonant inductor is provided.

2. Rectifier Diode Reverse Recovery with A Linear Resonant Inductor

The one switching loss that both FB-ZVS-PWM converter and ZVS-QRC do not avoid is the charging loss that results from the rectifier diode capacitance. Losses proportional to $1/2CV^2$ appear.

FB-ZVS-PWM converter with high voltage and power level requires special attention to parasitic that *can* affect its operation.

The ZVS converters use a resonant inductor ***(***Lr***)*** to achieve ZVS for the switches. The size of the inductor is determined by the load and input voltage range under which ZVS in maintained. To reduce the switching losses for a wide load and input voltage range, a large resonant inductance is required. However, for large value of Lr, the ringing frequency is low, causing higher diode voltage stress**,** higher snubber losses, and higher switching noise.

In the FB-ZVS-PWM the ringing across the rectifier diode is affected by the resonant inductance, the winding capacitance and the rectifier diode characteristics. This ringing across the rectifier *occurs* when the voltage rises in the secondary of the transformer, and the resonant inductance rings with the diode rectifier capacitance and the winding capacitances. Even though fast recovery rectifiers are employed, the diode reverse recovery ***can*** produce peak voltages higher than three times the voltage applied to the secondary.

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The ringing has to be snubbed, but the use of an RC snubber in parallel with the rectifier diode would introduce large losses since the ringing frequency is less than 10 times the switching frequency, ***f,*** due the larger value of Lr.

3. Rectifier Diode Reverse Recovery with A Saturable Resonant Inductor

It is shown that the incorporation of a saturable inductor to ZVS-QRCs and to the FB-ZVS-PWM converter results in a significant improvement in their performance.

The employment of a saturable resonant inductor can reduce parasitic oscillations between the diode junction capacitance and the resonant inductor. When in a linear resonant inductor is employed, the diode junction capacitance starts to resonate with the inductor, when the diode suffers from a prompt reverse voltage. The large resonant inductance produces low ringing frequency that increases the rectifier voltage stress and switching noise . Replacing the linear resonant inductor by a resonant inductor gets saturated, when the diode junction capacitance starts to resonant with it. The inductance versus current curve of a typical saturable inductor is shown in fig (1), where Ia is the critical saturable current.

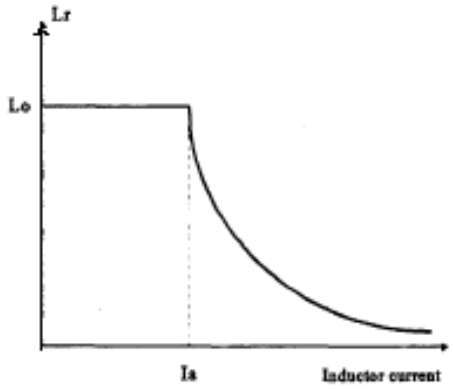


Fig 1. Inductor vs current of a saturable inductor

4. Simulation Results

In order to verify the results predicted theoretically, simulations have been done. A diode model, with reverse recovery, is necessary to obtain accurate simulation results to verify its behavior. The diode model employed is fully described. Some parameters are needed to build this model. A MURl530 (Motorola) fast recovery rectifier is tested in the laboratory and its reverse recovery curve obtained, is shown in Fig 2. The parameters necessary to build diode model are taken from Fig. 2.

In the Fig. 3 is shown the Buck-ZVS-QRC used in the simulations. Fig. 4(a) shows its simulation results with a linear resonant inductor, and Fig. 4(b) with a saturable resonant inductor. The saturable inductor model employed, in these simulations, is the Jiles-Atherton model.

The parameters used in the simulations are as follows:

Vi = 40V, Cr = 27nF, Io,= 10A
Lr = 6 μH (linear inductor)
Lo = 6 μH and Ia=4A (saturable inductor)
D_2 = MURI530 diode model.

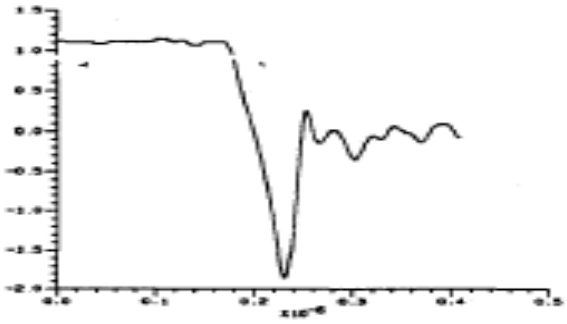


Fig. 2 Reverse recovery a a MUR1530 fast recovery rectifier

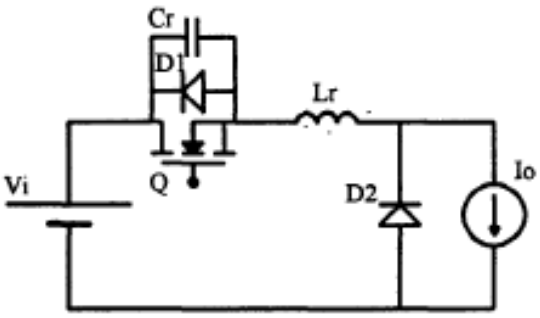


Fig. 3 Buck-ZVS-QRC

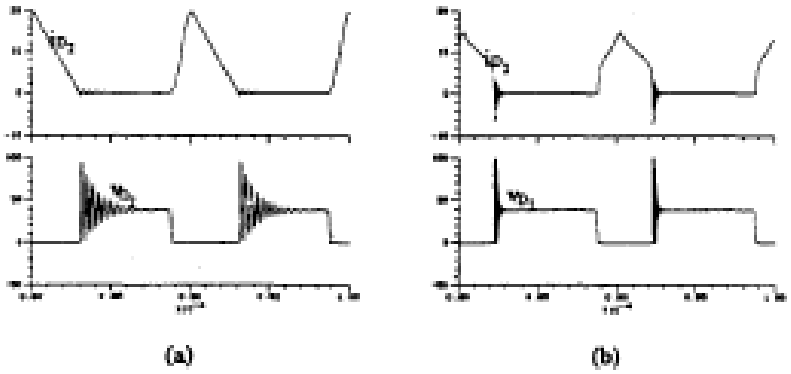


Fig. 4 Simulated reverse recovery of a MUR 1530 in a Buck-ZVS-QRC with: a). a linear resonant inductor, b). a saturable resonant inductor

It can be seen from the simulations that the parasitic oscillations are reduced, when a saturable resonant inductor is present in the circuit This reduction is due to the saturation of the resonant inductor when the reverse recovery occurs, and it has a much reduced resonant inductance. However, its reverse current is larger, because it is function of di/dt (dit/dt= Vi / Lr *).* In addition, the peak reverse voltage across the rectifier diode is greater.

5. Designing The Clamping Circuit with A Linear Resonant Inductor

A scheme has been proposed that clamps the maximum peak voltage of the ringing and returns part of the energy to the output or input. The design of the clamping circuit is based on balancing the charge transferred to the clamping capacitor, Cc, with the charge retuned to the output (or input) or the charge dissipated in Rc, in order to maintain the voltage across Cc constant.

This design procedure was developed for a Buck-ZVS-QRC, but it is also valid for the HB-ZVS-QRC and FB-ZVS-PWM converter, since that the circuit gets referred to secondary of the transformer . Buck-ZVS-QRC with the clamping circuit is shown in Fig. 5.

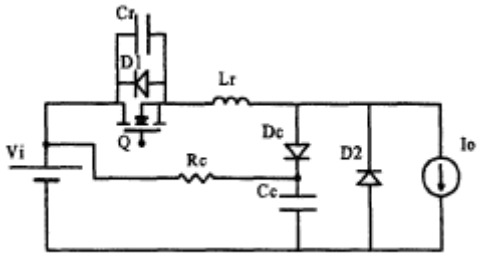


Fig. 5 Buck-ZVS-QRC with the clamping circuit

Figure *6* shows the incremental model and waveforms for charging of the rectifier junction capacitance, after adding the clamping circuit. The capacitor is the rectifier junction capacitance to the Buck-ZVS-QRC, HB-

ZVS-QRC and FB-ZVSPWM converter with a half-bridge rectifier in the secondary side. It is the parallel combination of the two rectifier junction capacitances, to the HB-ZVS-QRC and FB-ZVS-PWM converter with a full-bridge rectifier in the secondary side. The inductor is the resonant inductance or the resonant inductance plus the transformer's leakage inductance, and the resistor, Rp, represents the losses throughout the circuit. Capacitor Cc, must be large enough to be approximated by a constant voltage source, Vcp.

The rectifier diode capacitor is nonlinear. It varies inversely with the square root of its voltage. In the design of the clamping circuit is assumed a linear rectifier diode capacitor.

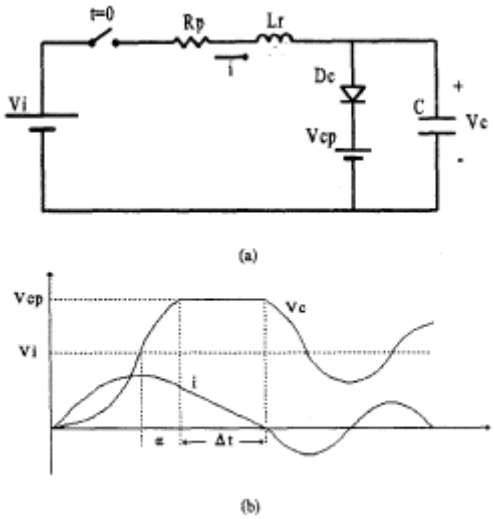


Fig. 6 Incremental model and waveforms for charging of the rectifier capacitance with clamping circuit added

The energy that flows into this clamping circuit *can* be calculated as follows. Defining α as the angle of the oscillation cycle from when the capacitor voltage passes through Vi, until the capacitor voltage reaches the clamp voltage, Vcp, then

$$\text{Sin } \alpha = (Vcp - Vi)/Vi = u \quad (1)$$

where u is a correction factor, so

$$\alpha = \arcsin(u) \quad (2)$$

The inductor current at the end of this period is

$$I(\alpha) = (Vi \cos \alpha)/\sqrt{(Lr/C)} = (Vi \sqrt{(1-u^2)} / \sqrt{(Lr/C)} \quad (3)$$

This Current decreases linearly with time, until it reaches zero. The duration of the clamping action is

$$\Delta t = (Lr\ I(\alpha)/ (Vcp - Vi) \quad (4)$$

and the energy flowing into the clamping circuit is therefore

$$E_{CP} = [\ I(\alpha).\ Vcp.\ \Delta t] / 2 = \{\{\ Lr\ I^2(\alpha)\}/ 2\}\ \{(1+u)/u\} \quad (5)$$

Substituting *I(a)* in to ***(5),*** it ***can*** be rewritten

$$E_{CP} = \{(C.\ Vi^2)/2\ \}\ \{(1+u)^2.(1-u)/\ u\} \quad (6)$$

This expression shows that the energy delivered to the clamping circuit equals the energy stored in the rectifier diode capacitor times a correction factor .

Not all the energy flowing into the clamping circuit must be lost. If the clamping circuit energy is discharged to the output (or input), then only a part of the clamping circuit energy is lost. The rest is delivered to the output (or input).

The Power flowing into the Clamping Circuit

$$P_{CP} = E_{CP}.f \quad (7)$$

The Resistor of the Clamping Circuit

a) If all the power flowing must be lost.

$$R_C = (Vcp^2 / P_{CP}) \quad (8)$$

b) If a part of the power flowing is recovered to a voltage source V.
The voltage source, V, *can* be the input voltage or the output voltage.

$$R_C = \{Vcp(Vcp - V\} / P_{CP} \quad (9)$$

The loss in the R_C is:

$$PRc = (Vcp - V)^2 / R_C \quad (10)$$

The recovered power to V is:

$$P_l = \{V(Vcp - V\} / R_C \quad (11)$$

The Capacitor of the Clamping Circuit.

As the capacitor must be large enough to be approximated by a constant voltage source, will be considered $R_C.C_C$ =400.T, where T is the switching period, then

$$C_C = (400.T) / R_C \quad (12)$$

6. Designing The Clamping Circuit with A Saturable Resonant Inductor

The main difference between the design of the clamping circuit with a linear inductor and with a saturable inductor is that at the instant when the rectifier diode reverse recovery occurs the resonant inductor is saturated and its inductance is much reduced. During the rectifier diode capacitance charging the inductor current is Io + i , where Io, is the output current and i is the current that flows in the rectifier diode capacitance. So, when reverse recovery begins the saturated inductance is given by:

$$Lr = L (Io + i) \quad (13)$$

Applying same procedure as used in the clamping circuit design with a linear resonant inductor, gives:

$$I(\alpha) = (Vi \cos \alpha)/ \sqrt{\{L(Io + i)/C\}} = (Vi \sqrt{(1-u^2)} / \sqrt{\{L(Io + i)/C} \quad (14)$$

Duration of the Clamping Action.

$$dt = \{L(Io + i). di\} / (Vcp - Vi) \quad (15)$$

Considering the inductance represented by its more classical expression, that is shown in (17).

$$L_r = L_o . \text{sech}^2 (L_o/\Phi_S). i \quad (16)$$

where Φ_S is the saturation flux.
So, the current and the energy flowing into the clamping circuit are given by:

$$I(\alpha) = \{Vi . \sqrt{(1- u^2)}/ \sqrt{(L_o /C)}\}. \cos h \{(L_o/\Phi_S)(Io + I(\alpha))\} \quad (17)$$

If Vi, L_o, C, Φ_S and Io are known, the transcendental equation can be resolved to I(α). With I(α) determined, E_{CP} is computed and the rest of the clamping circuit design has the same procedure as applied with a linear resonant inductor.

7. Experimental Results

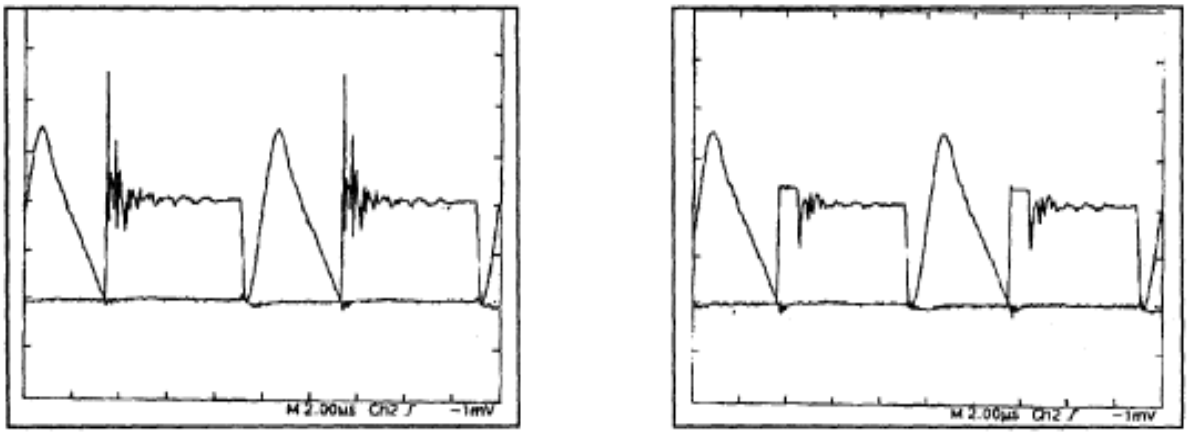
Prototypes have been built and tested in the laboratory to confirm the results predicted theoretically and by simulation.

Buck-ZVS-QRC with a Linear Resonant Inductor:

The power stage diagram is shown in Fig**.** 5 and the parameters are the following:

Vi = 40V, Cr = 27nF, f= 100kHz
Lr = 6µH Q =IRF640 (International rectifier)
D_2 = MURI530 (Motorola), C= 200 pF at VD_2 = 40V.

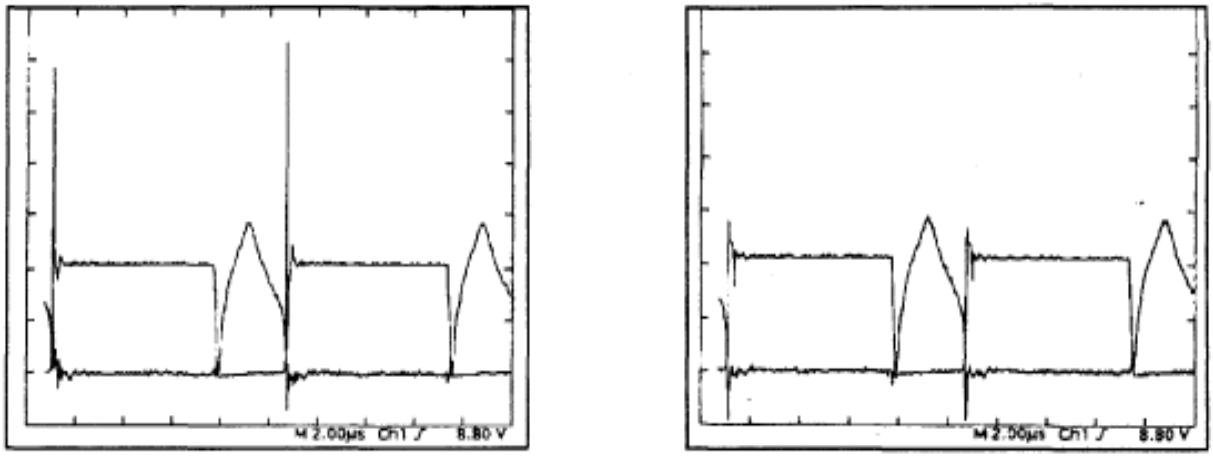
Adopting V=50V, the calculation of the components of the clamping circuit follows the design procedure related in the section V. So, the power flowing into the clamping circuit is P_{CP} = 0.75mW



a. b.

Fig.7 Experimental of the waveforms of the Buck ZVS-QRC with a linear resonant inductor, a) without a clamping circuit, b) with a clamping circuit at Ip=10A (scales voltage 20V/div, current 2A/div, Time 2µs/div)

With the value of P_{CP} determined, the resistor and the capacitor of the clamping circuit are the following R_C=39kΩ and C_C=120nF. Figure 7, shows the current and voltage waveforms of the rectifier diode, obtained experimentally. In Fig. 7(a), is shown its waveforms without the clamping circuit and in Fig. 7(b) with the clamping circuit.



a. b.

Fig. 8 Experimental of the waveforms of the Buck ZVS-QRC with a saturable resonant inductor, a) without a clamping circuit, b) with a clamping circuit at Ip=10A (scales voltage 20V/div, current 2A/div, Time 2µs/div)

Buck-ZVS-QRC with a Saturable Resonant Inductor

All parameters are the same used with the linear resonant inductor, except the resonant inductor. In this case a saturable resonant inductor is employed with the following parameters: Φ_S= 37μWb, Lo = 6 μH and Ia=4A, and Lr = 4 tums on E-20 ungapped core (Thorton).

Adopting Vcp = 50V, the calculation of the components of the clamping circuit follows the design procedure described in the section VI. The worst case occurs with rated current, because with this condition the inductance is saturated (minimum value). So, the clamping circuit's design is done with rated current. The power flowing into the clamping circuit is P_{CP} = 78mW. As the value of P_{CP} is close to the value found with a linear inductor, the values of the resistor and the capacitor are the same.

Current and voltage waveforms of the rectifier diode are shown in Fig. 8. Fig. 8(a) shows its waveforms without a clamping circuit and Fig. 8(b) with the clamping circuit. As can be seen in Fig. 7 and 8, the current and voltage waveforms obtained experimentally agree with the design done in the previous section.

8. Conclusion

An analysis of the effects of the saturable inductor on the reverse recovery of the rectifying diode of ZVS converters is presented. The clamping circuit with a linear inductor is shown and compared with the design of the clamping circuit with a linear inductor. The experimental results obtained agree with the predicted theoretically. It can be affirmed that the energy flowing into the clamping circuit is practically the same in both cases, because this energy proceeds from the diode junction capacitance. The saturation of the resonant inductor results in a substantial reduction of the parasitic oscillations. However, the peak current and the peak voltage during the reverse recovery are larger than the case with a linear inductor.

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