

## A novel impedance source fed H-type flying capacitor multilevel inverter

C. R. Balamurugan, P. Vijayakumar, T. Sengolrajan

Department of EEE, Karpagam College of Engineering, India

---

### Article Info

#### Article history:

Received Apr 23, 2019

Revised Jun 7, 2019

Accepted Jul 14, 2019

---

#### Keywords:

Five level

Impedance source

MLI

Stepped wave

THD

THI

Trapezoidal

---

### ABSTRACT

In this paper, simulation using MATLAB/SIMULINK is performed with bipolar triangular fixed amplitude multi-carrier Phase Disposition (PD) PWM strategy with sine wave, Third Harmonic Injection, 60-degree Pulse Width Modulation and stepped wave reference for the chosen impedance Source based H-Type flying capacitor Multilevel Inverter (ISBH-Type FCMLI). The root means square value of the fundamental component and Total Harmonic Distortion of the output voltage which are the most important performance indices for the chosen inverter topologies are evaluated presented and compared for various references through duty ratios. From the simulation results it is observed that for various references the THD is almost similar but the root mean square value in terms of voltage is more for THI, 60-degree PWM and stepped wave reference with phase disposition strategy. The results are obtained for  $m_a$  (amplitude modulation index)  $< 1$  (under amplitude modulation index),  $m_a=1$  (normal amplitude modulation index) and  $m_a > 1$  (over amplitude modulation index).

*Copyright ©2019 Institute of Advanced Engineering and Science.  
All rights reserved.*

---

### Corresponding Author:

C. R. Balamurugan,

Department of EEE,

Karpagam College of Enigneering,

Myleripalayam Village, Othakkal Mandapam, Tamil Nadu 641032, India.

Email: crbalain2010@gmail.com

---

## 1. INTRODUCTION

Multilevel Inverter (MLI) is made up of multiple switches. Multilevel inverter [1] enables the use of environmental friendly energy sources like solar cells and fuel cells. The main feature of this MLI is its ability to reduce the voltage stress on each power device due to the utilization of multiple levels on the DC bus. Two switches of the same leg cannot be switched ON simultaneously which will lead to short circuit. It has very narrow output voltage range. Boosting of output is not possible. I.e the output side voltage is less than or equal to the input side voltage. Related gate drive is required for each switch. Provides second order filter, suppresses current and voltage ripples. Impedance source inverter has both inductor and capacitor in the dc link it provides constant high impedance voltage source. It provides impedance source coupling to the inverter on one port and DC source on other port. It's a Transformer less network, so simple. A detailed literature survey was made on the proposed work [1-28]. Based on the diffeternt author works the study is made and identified the problems. The solution for the problems was focused to address the issue. The proposed work will be used for both static and dynamic loads applications like drives [7, 14].

## 2. IMPEDANCE SOURCE FED MULTILEVEL INVERTER

Figure 1 displays the traditional inveter. The conventional system will give only less number of voltage levels with more amount of distortion in the supply [2]. Figure 2 shows the need for boosting the input voltage. Combination of passive elements is used to boost or buck the output. Figure 3 gives

the impedance network fed to the inverter circuit. The special type of switches used as bidirectional switches. Figure 4 displays the H-type FCMLI. Table 1 shows H-type flying capacitor multilevel inverter.

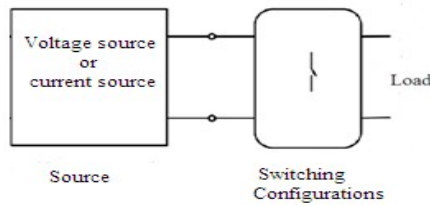


Figure 1. Traditional multilevel inverter

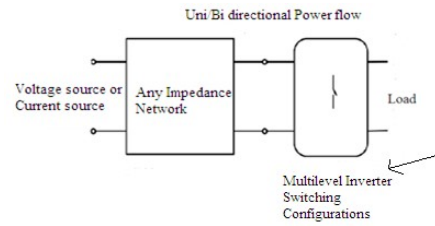


Figure 2. Impedance network fed multilevel inverter

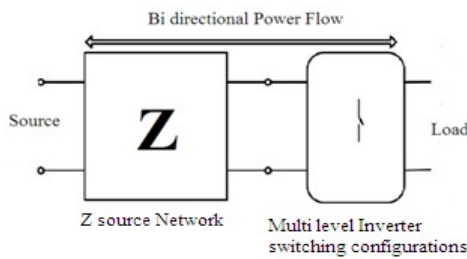


Figure 3. Z source fed multilevel inverter

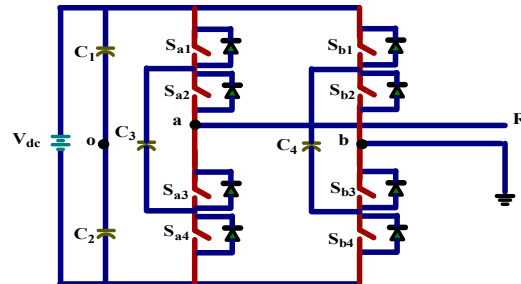


Figure 4. H-type FCMLI

Table 1. H-type flying capacitor multilevel inverter - switch states and output voltage levels

S <sub>a1</sub>	S <sub>a2</sub>	S <sub>a3</sub>	S <sub>a4</sub>	S <sub>b1</sub>	S <sub>b2</sub>	S <sub>b3</sub>	S <sub>b4</sub>	V <sub>ao</sub>	V <sub>bo</sub>	V <sub>ab</sub> =V <sub>RN</sub>
0	0	1	1	1	1	0	0	-1/2 V <sub>dc</sub>	1/2V <sub>dc</sub>	-V <sub>dc</sub>
0	0	1	1	0	1	0	1	-1/2 V <sub>dc</sub>	0	-1/2 V <sub>dc</sub>
0	1	0	1	1	1	0	0	0	1/2 V <sub>dc</sub>	-1/2 V <sub>dc</sub>
1	0	1	0	1	1	0	0	0	-1/2 V <sub>dc</sub>	1/2 V <sub>dc</sub>
1	1	0	0	1	1	0	0	1/2 V <sub>dc</sub>	1/2 V <sub>dc</sub>	0
0	0	1	1	0	0	1	1	-1/2 V <sub>dc</sub>	-1/2 V <sub>dc</sub>	0
0	1	0	1	0	0	1	1	0	-1/2 V <sub>dc</sub>	-1/2 V <sub>dc</sub>
1	1	0	0	0	1	0	1	1/2 V <sub>dc</sub>	0	1/2 V <sub>dc</sub>
1	0	1	0	0	0	1	1	0	-1/2 V <sub>dc</sub>	1/2 V <sub>dc</sub>
1	1	0	0	0	0	1	1	1/2 V <sub>dc</sub>	-1/2 V <sub>dc</sub>	V <sub>dc</sub>

### 3. MODULATION SCHEME

The gate pulse is generated by comparing the reference signal with carrier frequency. The scheme developed based on CFD technic (Control Freedom Degree) [25]. Figure 5 shows the carrier arrangement of sinusoidal, third harmonic, 60 degree and stepped wave reference with phase disposition carrier.

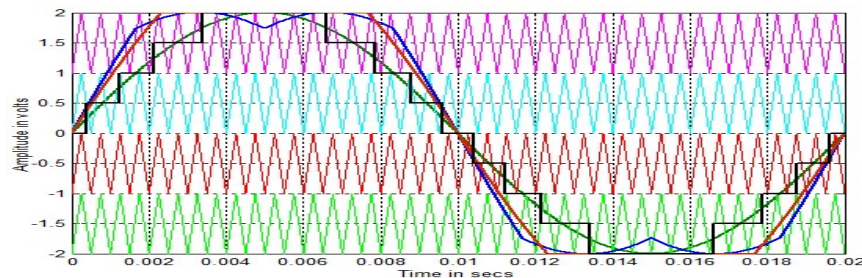


Figure 5. Sample carrier arrangement of sinusoidal, third harmonic, 60 degree and stepped wave reference with phase disposition carrier

#### 4. Z-SOURCE BASED MULTILEVEL INVERTER

Figure 6 shows the basic view of impedance source based H type flying capacitor multilevel inverter. The choice of multilevel inverter depends on the applications. This combination of Z source and multilevel inverter provides unique features [27-28]. Z source multilevel inverter [15, 17-24] composed of DC source, Z network and single H bridge inverter [26]. Figure 6 displays the power circuit of Z source based multilevel inverter. Voltage stress problem in conventional Z source inverter is overcome by Z source multilevel inverter. Voltage source and current source inverters can either buck or boost the voltage but Z source based multilevel inverter can able to both buck and boost the given voltage. Figure 6 shows the cascaded five level Z-source based multilevel inverter (ZSMLI). It has separate DC sources for each module with same voltage level. Presence of impedance network between DC source and main circuit overcome the limitations of traditional inverters. In traditional voltage source inverter the AC output voltage is below the DC input voltage and the dead time has to be introduced for both upper and lower devices which lead to distortion of output waveform. But the Z-source multilevel inverter can buck and boost the given input voltage.

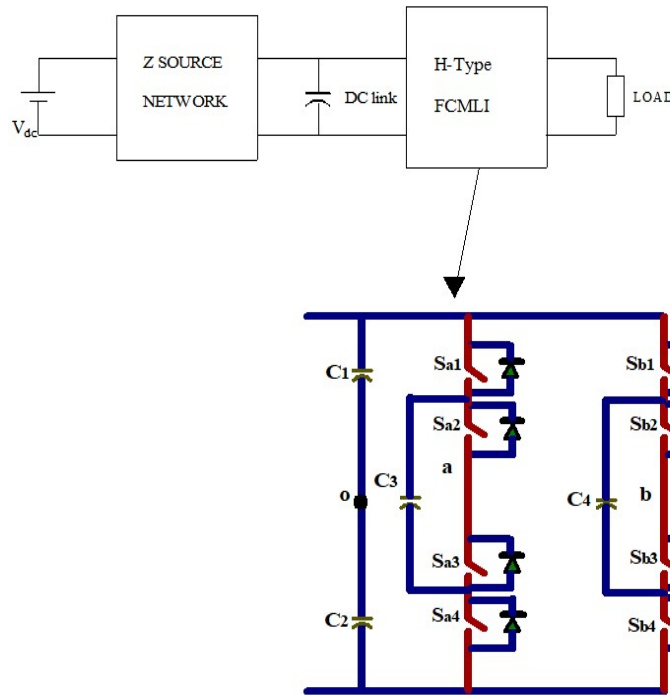


Figure 6. Z-source based multilevel inverter

#### 5. SIMULATION RESULTS

The simulated output voltage is shown for only one sample value of  $m_a=1$ . The following parameter values are used for simulation:  $V_{dc} = 100V$ ,  $R(\text{load}) = 10 \text{ ohms}$ ,  $C_1 = C_2 = C_3$  and  $C_4 = 1000 \text{ e-3 Farad}$ ,  $f_c = 2000 \text{ Hz}$  and  $f_m = 50 \text{ Hz}$ . Figures shows the sample five level output voltage generated by PDPWM [10,12] strategy with sine, THI, 60 degree and stepped wave reference and its FFT plot is shown in below Figures. Table 3 to Table 6 show the comparison of %THD,  $V_{RMS}$  (fundamental),  $V_{\text{peak}}$  and DC component for PDPWM strategies with various references.

##### 5.1. Impedance source multilevel inverter with sine reference

Figure 7 (a) and Figure 7 (b) represent the output voltage and harmonic spectrum of Z-source based H-type FCMLI for sinusoidal reference with PDPWM Strategy [16]. An output voltage and THD obtained are shown in Figure 7 (a).

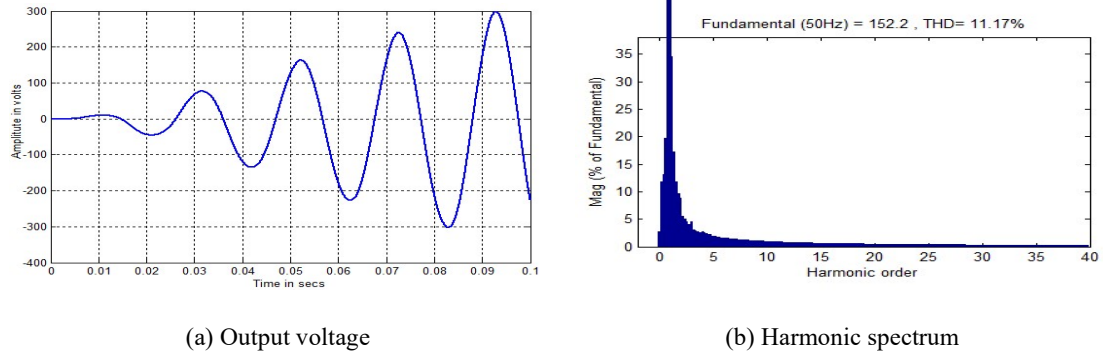


Figure 7. Impedance source multilevel inverter with sine reference

**5.2. Impedance source multilevel inverter with THI reference**

Figure 8 (a) and Figure 8 (b) show the output voltage waveform and harmonic spectrum of Z-source based H-type FCMLI for THI reference [11, 13] with PDPWM Strategy. An output voltage and THD are obtained that is shown in Figure 8 (a) and Figure 8 (b).

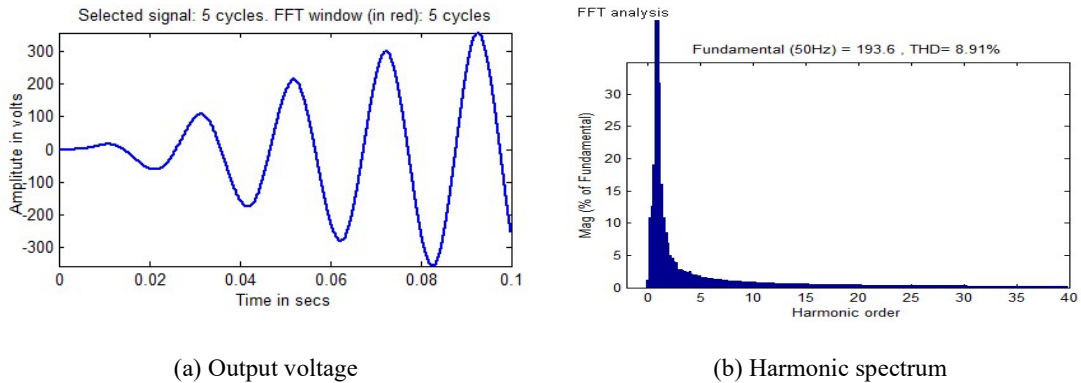


Figure 8. Impedance source multilevel inverter with THI reference

**5.3. Impedance source multilevel inverter with 60 degree reference**

Figure 9 shows the output voltage and harmonic spectrum of Impedance Source multilevel Inverter with 60 degree reference. An output voltage and THD are obtained which shown in Figure 9 (a) and Figure 9 (b).

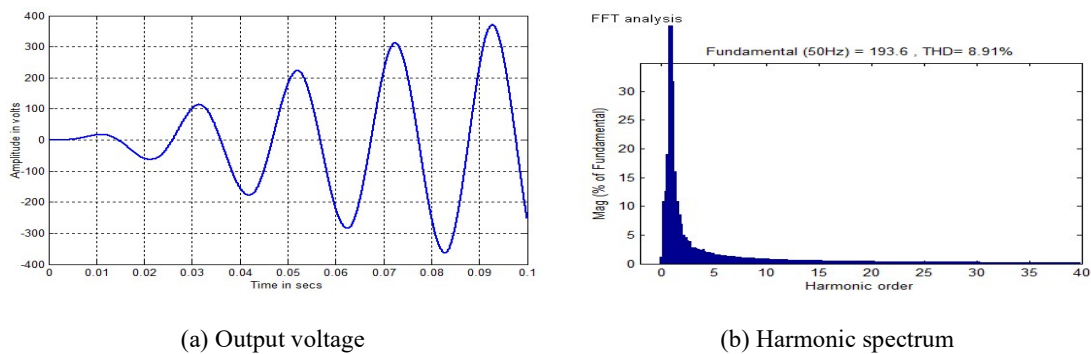


Figure 9. Sample FFT plot for impedance source multilevel inverter with 60 degree reference

**5.4. Impedance source multilevel inverter with stepped wave reference**

Figure 10 displays the output voltage and harmonic spectrum of Impedance Source multilevel Inverter with stepped wave reference. An output voltage and THD is obtained which shown in Figure 10 (a) and Figure 10 (b).

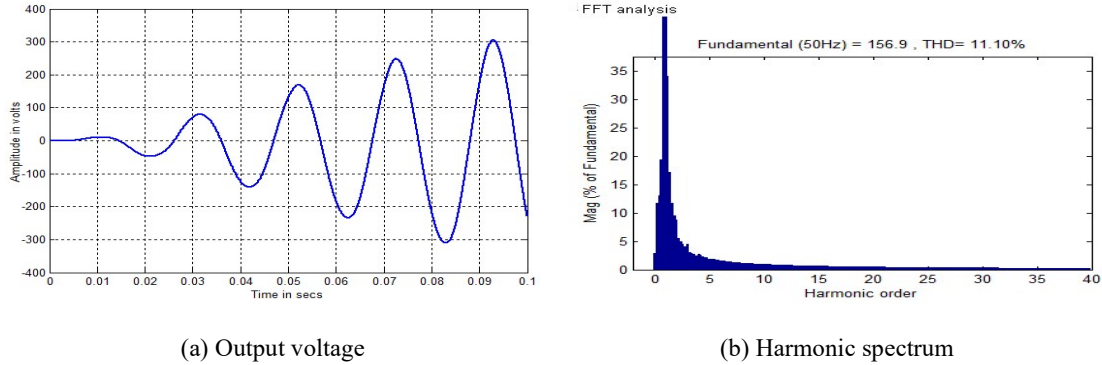


Figure 10. Impedance source multilevel inverter with stepped wave reference

In this analyse presence of RMS output voltage and THD in the output waveform is observed for various topologies by varying modulation index. The following tables represent measurements across multilevel inverter. Table 2 shows the simulation values. Table 3 and Table 4 show the measurement across MLI for  $L = 3\text{mH}$ ,  $C = 4700\mu\text{F}$  and  $L = 3\text{mH}$ ,  $C = 470\mu\text{F}$ . Table 5 and Table 6 represent the measurement across MLI for  $L = 250\mu\text{H}$ ,  $C = 500\mu\text{F}$  and  $L = 160\mu\text{H}$ ,  $C = 1000\mu\text{F}$ .

Table 2. Simulation values chosen

Component	Values Chosen
Input Voltage	100 V
Impedance Network	$L_1 = 3\text{mH}$
	$L_2 = 3\text{mH}$
	$C_1 = 4700\text{ micro farad}$ $C_2 = 4700\text{ micro farad}$
H-Type FCMLI	Bus Capacitor ( $C_1$ ) = $1000e^{-6}$
	Bus Capacitor ( $C_2$ ) = $1000e^{-6}$
	MOSFET
AC Filter	Clamping capacitor $C_1 = C_2 = 100\text{ e}^3$
	$L = 3e^{-3}\text{ H}$ $C = 4700e^{-6}$
Load	$R = 10\text{ ohm}$

Table 3. Output voltage THD for various modulation indices

Modulation Type	Modulation Index	Sine Reference	THI Reference	60 degree Reference	Stepped wave reference
Over Modulation Index ( $m_a > 1$ )	1.4	9.11	8.26	8.38	8.89
	1.3	9.39	8.33	8.40	9.16
	1.2	9.76	8.38	8.52	9.83
Normal Modulation Index ( $m_a = 1$ )	1.1	10.27	8.44	8.71	10.48
	1	7.78	9.02	8.91	11.10
	0.9	7.54	10.69	10.40	12.48
Under Modulation Index ( $m_a < 1$ )	0.8	15.63	13.05	13.06	14.96
	0.7	17.26	14.66	14.67	16.75
	0.6	18.45	15.98	16.83	18.76

Table 4.  $V_{rms}$  (fundamental) output voltage for various modulation indices

Modulation Type	Modulation Index	Sine Reference	THI Reference	60 degree Reference	Stepped wave reference
Over Modulation Index ( $m_a > 1$ )	1.4	135.2	141.8	141.1	135.8
	1.3	132.4	141.6	140.8	133
	1.2	127.9	141.1	140	125.7
	1.1	121	140.2	138.6	118.3
Normal Modulation Index ( $m_a = 1$ )	1	87.96	132.5	136.9	111
	0.9	80.73	105.3	112.8	86.84
Under Modulation Index ( $m_a < 1$ )	0.8	52.63	71.9	76.9	55.99
	0.7	31.53	46.33	50.76	33.24
	0.6	28.78	28.62	24.97	15.66

Table 5.  $V_{peak}$  output voltage for various modulation indices

Modulation Type	Modulation Index	Sine Reference	THI Reference	60 degree Reference	Stepped wave reference
Over Modulation Index ( $m_a > 1$ )	1.4	191.2	200.6	199.6	192.1
	1.3	187.2	200.2	199.1	188.1
	1.2	180.9	199.5	198	177.7
	1.1	171.2	198.3	196.1	167.2
Normal Modulation Index ( $m_a = 1$ )	1	124.4	187.4	193.6	156.9
	0.9	114.2	148.9	159.5	122.8
Under Modulation Index ( $m_a < 1$ )	0.8	74.5	101.7	108.7	79.18
	0.7	44.59	65.52	71.79	47.01
	0.6	30.52	48.21	35.31	22.15

Table 6. DC component output voltage for various modulation indices

Modulation Type	Modulation Index	Sine Reference	THI Reference	60 degree Reference	Stepped wave reference
Over Modulation Index ( $m_a > 1$ )	1.4	0.90	2.87	2.29	1.57
	1.3	0.66	2.94	2.33	0.97
	1.2	0.08	2.24	1.95	0.79
	1.1	0.95	1.95	1.47	2.10
Normal Modulation Index ( $m_a = 1$ )	1	2.37	1.65	1.19	2.80
	0.9	7.54	3.99	3.73	6.35
Under Modulation Index ( $m_a < 1$ )	0.8	13.54	13.67	12.57	12.24
	0.7	15.84	17.45	16.40	14.06
	0.6	17.98	21.09	19.99	16.99

## 6. CONCLUSION

The performance of Impedance source based flying capacitor multilevel Inverter with sinusoidal, third harmonic injection, 60 degree and stepped wave reference and PDPWM strategy are analysed in this work. Simulation was carried out for the proposed topologies using PWM technique. RMS values of output voltage and THD are observed using FFT analysis in MATLAB/Simulink environment. From the analysis of each proposed topology by varying impedance network values (L and C) are developed. From the simulation results it is found that for different references the THD is almost similar but the root mean square value in terms of voltage is more for THI, 60 degree PWM and stepped wave reference with phase disposition strategy. The results are observed for various values of  $m_a$  (Amplitude Modulation Index) like under amplitude modulation index, normal amplitude modulation index and over amplitude modulation index.

## REFERENCES

- [1] Rodriguez, J.S. Lai, and Fang Z. Peng, "Multilevel Inverters: A Survey of Topologies, Controls and Applications," *IEEE Trans on Industrial Electronics*, vol. 49(4), pp. 724-738, 2002.
- [2] J. S. Lai and F. Z. Peng, "Multilevel converters – A new breed of power converters," *IEEE Transactions Industry Applications*, vol. 32, pp. 509-517, 1996.
- [3] Leon M. Tolbert and T.G. Habetler, "Novel multilevel inverter carrier-based PWM methods," *IEEE IAS Annual meeting*, pp. 1424-1431, 1998.
- [4] Li Li, Yaguang Liu, and Pragasen Pillay, "Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters," *IEEE Trans. on Industry Applications*, vol. 36(1), pp. 160-170, 2002.

- [5] Brendan Peter McGrath and Donald Grahame Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 49(4), 2002.
- [6] P.C. Loh, D.G. Holmes, and T.A. Lipo, "Synchronization of distributed PWM cascaded multilevel inverters with minimal harmonic distortion and common mode voltage," *Proc. IEEE PESC*, pp. 177-182, 2003.
- [7] D. Krug, S. Bernet, and S. Saeed Fazel, "Comparison of 2.3-kV medium-voltage multilevel converters for industrial medium-voltage drives," *IEEE transactions on Industrial Electronics*, vol. 54(6), 2007.
- [8] M. Ghasem Hosseini Aghdam, S. Hamid Fathi, and B. Gharehpetian, "Harmonic optimization techniques in multi-Level voltage-Source inverter with unequal DC sources," *Journal of Power Electronics*, vol. 8(2), 2008.
- [9] Zhong Du, M. Tolbert, B. Ozpineci, and N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 24(1), 2009.
- [10] Palanivel P and S. Sekher, "Phase Shifted Carrier Pulse Width Modulation for Three Phase Multilevel Inverter to Minimize THD and Enhance Output Voltage Performance," *Journal of Electrical Systems*, vol. 6(2), pp. 1-13, 2010.
- [11] Bambang Sujanarko, "Advanced carrier based Pulse Width Modulation in asymmetric cascaded multilevel inverter," *International Journal of Electrical & Computer Sciences*, vol. 10(6), 2010.
- [12] Hussein A. Konber and Osama I. EL-Hamrawy, "Implementing a three phase nine-level cascaded multilevel inverter with low harmonics values," *ProcsMEPCON'10, Cairo University, Egypt, December 19-21, 2010*.
- [13] Faete Filho, Leon M. Tolbert, Yue Cao and Burak Ozpineci, "Real-time selective harmonic minimization for multilevel inverters connected to solar panels using artificial neural network angle generation," *IEEE Transactions on Industry Applications*, vol. 47(5), pp. 2117-2124, 2011.
- [14] Ashrafi B, Niroomand M, and Ashrafi Nia, "Novel reduced parts on-line uninterruptible power supply," *Procs IEEE 2012 International Power Engineering and Optimization Conference*, pp. 252-257, 2012.
- [15] Yushan Liu, Baoming Ge, Haitham Abu-Rub, Fang ZhengPeng, "A modular multilevel space vector modulation for photovoltaic quasi-Z-Source cascade multilevel inverter," *Proceedings of Twenty-Eighth Annual IEEE Conference on Applied Power Electronics APEC and Exposition*, pp. 714-718, 2013.
- [16] Yushan Liu, Baoming Ge, Haitham Abu-Rub, Fang ZhengPeng, "Phase-shifted pulse-width-amplitude modulation for quasi-Z-source cascade multilevel inverter-based photovoltaic power system," *IET Power Electronics*, vol. 7(6), pp. 1444-1456, 2014.
- [17] B. Manjunatha, "Advanced Pulse Width Modulation Techniques for Z Source Multi Level Inverter," *International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering*, vol. 9(3), pp. 359-364, 2015.
- [18] M. Trabelsi, H. Abu-Rub, and BaomingGe, "1-MW quasi-Z-source based multilevel PV energy conversion system," *Proceedings of IEEE International Conference on Industrial Technology (ICIT)*, pp. 224-229, 2016.
- [19] K. Vijayalakshmi and C.R. Balamurugan, "A Review on Z-Source Based Multilevel Inverter with Reduced Number of Switches," *2016 International Conference on Engineering and Technology (ICET). Karpagam College of Engineering, Coimbatore, December 16-17, 2016*.
- [20] K. Vijayalakshmi and C. R. Balamurugan, "Investigations on Z-source based cascaded five level inverter," *International Journal of Signal Processing, Image Processing and Pattern Recognition*, vol. 9(12), pp. 37-50, 2016.
- [21] K. Vijayalakshmi and C. R. Balamurugan, "Simulation and Analysis of Improved Switched Inductor Quasi Z-Source Based Multilevel Inverter with Reduced Number of Switches," *International Conference on Emerging Trends in Science, Engineering & Technology, Jerusalem College of Engineering, Chennai, March 18-19, 2017*.
- [22] S.M. Revathi and C.R. Balamurugan, "A Review on Various Z-Source Fed Multilevel Inverter," *10th International Conference on Recent Innovations in Science, Engineering and Management, Dhruva Institute of Engineering and Technology, Nalgonda, July 7, 2017*.
- [23] K. Vijayalakshmi and C.R. Balamurugan, "Z Source Multilevel Inverter Based on Embedded Controller," *TELKOMIKA Indonesian Journal of Electrical Engineering and Computer Science*, vol. 6(1), pp. 1-8, 2017.
- [24] C.R. Balamurugan and K. Vijayalakshmi, "Comparative Analysis of Various Z-source Based Five Level Cascaded H-bridge Multilevel Inverter," *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 7(1), pp. 1-14, 2018.
- [25] C.R. Balamurugan and R. Bensraj, "Analysis of Various Carriers Overlapping PWM Strategies for a Single Phase Ternary Multilevel Inverter," *International Journal of Applied Power Engineering*, vol. 7(1), pp. 27-39, 2018.
- [26] C.R. Balamurugan, S.P. Natarajan, V. Padmathilagam, and T.S. Anandhi, "Design of a New Three Phase Hybrid H-bridge and H-Type FCMLI for Various PWM Strategies," *International Journal of Advances in Applied Science (IAAS)*, vol. 4(3), pp. 82-89, 2015.
- [27] C.R. Balamurugan, S.P. Natarajan, and T.S. Anandhi, "Performance Evaluation of 3 $\Phi$  Asymmetrical MLI with Reduced Switch Count," *TELKOMIKA Indonesian Journal of Electrical Engineering and Computer Science*, vol. 3(3), pp. 671-680, 2015.
- [28] C.R. Balamurugan, S.P. Natarajan, T.S. Anandhi, and R. Besnraj, "Hardware Implementation of Cascaded Hybrid Multilevel Inverter with Reduced Number of Switches," *TELKOMIKA Indonesian Journal of Electrical Engineering and Computer Science*, vol. 3(2), pp. 314-322, 2016.