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Power System Performance Improvement by Optimal Placement and Sizing of SVC using Genetic Algorithm

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ABSTRACT

The power system loss minimization becomes more important as the need of power generation is more recent days. The loss minimization improves the voltage profile which improves the loadability of the system. In many types of flexible AC transmission system (FACTS) devices static var compensators (SVC) are cost vise it is affordable and it improves the system performance with lesser size. Here SVC is optimally placed in a test system of 30 bus system. Genetic algorithm is used to find the optimal results.

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1. INTRODUCTION

As the growth of complex electrical power network increases, a new approach called flexible alternating current transmission system (FACTS) has been implemented to increase the capability of the existing transmission systems. Through this approach, new power electronic controllers with high current, high voltage were introduced to control voltage level and power flows on transmission system without decreasing the system stability and security [1-3].

Hingorani, as the pioneer has put forward FACTS, and aimed to transport the control technology based on thyristor into the AC system. FACTS is adopted modern power electronics application at the important location of the transmission system in order to control and adjust one or more of the main parameters of the transmission system, to enhance the value of ac transmission assets. These parameters include voltages, impedance, phase angle, current, active power and reactive power. The application of FACTS proved that the technology brings many benefits to the world and there are many areas of improvement. In the meantime, current researches are focused to increase its effectiveness [4].

FACTS involve reliable and high-speed power electronic switches instead of mechanically controlled devices. FACTS is also supported by advances in digital protective relays, digital controls, integrated communications and advanced control centers. The heart of FACTS is thyristors: small, high voltage, semiconductor based devices that can switch electricity at mega-watt levels within milliseconds [5-7].

Here cost-effective SVC devices which are used to improve the voltage stability if placed optimally it reduces the loss also is used as FACTS device for improving voltage profile and reducing the losses.

2. PROBLEM DEFINITION

2.1. SVC modeling

Figure 1 shows equivalent circuit of an SVC connected to a terminal. The SVC is modeled by a shunt variable admittance and can be placed either at the terminal bus of a transmission line or in the middle of a long line. Considering the SVC without losses, the admittance only has its imaginary component and it can take values in a specified range (usually between 0 and the maximum SVC capacity studied, here 5 MVAr). This is denoted by:

$$y_{svc} = jb_{svc} \tag{1}$$

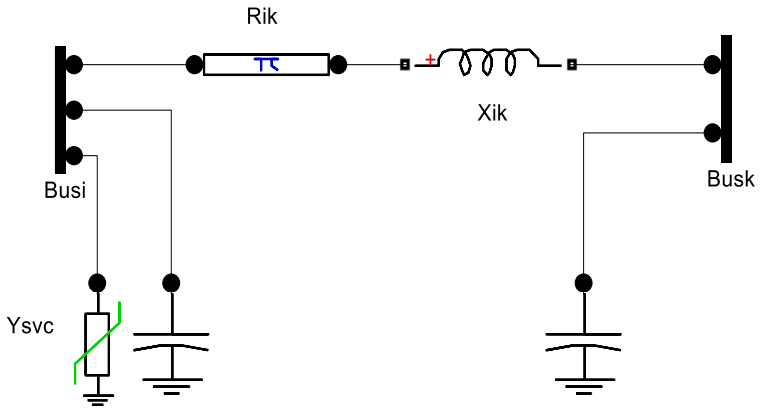

Figure 1. Equivalent circuit of an SVC connected to a terminal

In this case, only one term of the nodal admittances matrix is modified, corresponding to the node where the SVC is connected:

$$Y_{ii} = Y_{ii} + Y_{svc} \tag{2}$$

So, the Ybus matrix matrix modified as below

$$[Y_{bus}] = \begin{pmatrix} y_{ik} + \frac{y_{ik0}}{2} + y_{svc} & \cdots & -y_{ik} \\ \vdots & \ddots & \vdots \\ -y_{ik} & \cdots & y_{ik} + \frac{y_{ik0}}{2} \end{pmatrix} \tag{3}$$

Here

y_{ik}–admittance value of bus i to k
y_{ik0}-compensator admittance
y_{svc}–SVC admittance value
Y_{ii}–self admitance
The above ybus matrix is taken in power flow analysis for calculation of objective function.

2.2. Objective function

The objective function is power system loss minimization, which is given below

Minimize
Total Loss

$$=\sum_{l=1}^{n} I_l^2 R_l \tag{4}$$

$$=\sum_{l=1}^{n} [\, V_i^2 + V_j^2 - 2V_iV_j\cos(\delta_i - \delta_j)]Y_{ij}\cos\varphi_{ij} \tag{5}$$

Where,

n-number of branches
l-line number
Vi–sending end voltage
Vj–receiving end voltage
δi–sending end voltage angle
δj–receiving end voltage angle
Yij–sending end to receiving end line admittance

2.3. Constraints

Y_{svc} limits

$$Y_{svc\,min} \leq Y_{svc} \leq Y_{svc\,max} \quad (6)$$

$$V_{i\,min} \leq V_i \leq V_{i\,max} \quad (7)$$

3. GENETIC ALGORITHM

A genetic algorithm is a probabilistic search technique that computationally simulates the process of biological evolution. It mimics evolution in nature by repeatedly altering a population of candidate solutions until an optimal solution is found.

The GA evolutionary cycle starts with a randomly selected initial population. The changes to the population occur through the processes of selection based on fitness, and alteration using crossover and mutation. The application of selection and alteration leads to a population with a higher proportion of better solutions. The evolutionary cycle continues until an acceptable solution is found in the current generation of population, or some control parameter such as the number of generations is exceeded. Figure 2 shows genetic algorithm evolutionary cycle.

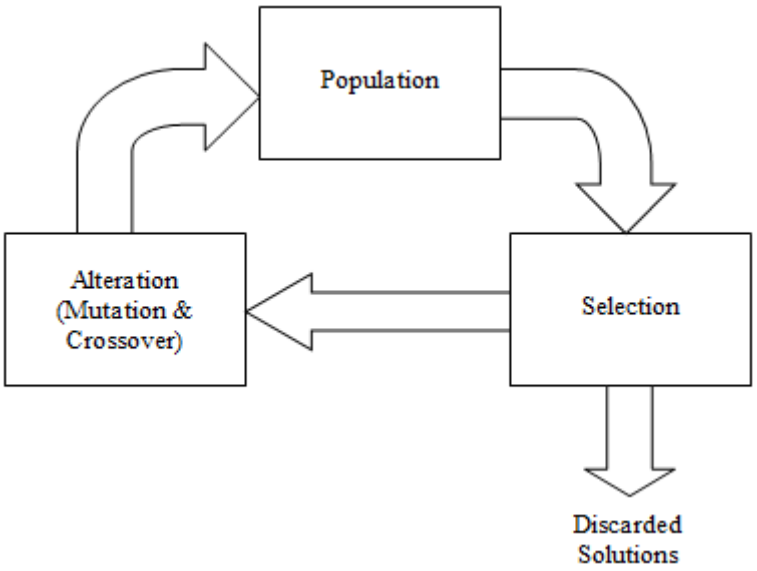

Figure 2. Genetic algorithm evolutionary cycle

The smallest unit of a genetic algorithm is called a gene, which represents a unit of information in the problem domain. A series of genes, known as a chromosome, represents one possible solution to the problem. Each gene in the chromosome represents one component of the solution pattern.

The most common form of representing a solution as a chromosome is a string of binary digits. Each bit in this string is a gene. The process of converting the solution from its original form into the bit string is known as coding. The specific coding scheme used is application dependent. The solution bit strings are decoded to enable their evaluation using a fitness measure.

In biological evolution, only the fittest survive and their gene pool contributes to the creation of the next generation. Selection in GA is also based on a similar process. In a common form of selection, known as

fitness proportional selection, each chromosome's likelihood of being selected as a good one is proportional to its fitness value.

The alteration step in the genetic algorithm refines the good solution from the current generation to produce the next generation of candidate solutions. It is carried out by performing crossover and mutation.

Crossover may be regarded as artificial mating in which chromosomes from two individuals are combined to create the chromosome for the next generation. This is done by splicing two chromosomes from two different solutions at a crossover point and swapping the spliced parts. The idea is that some genes with good characteristics from one chromosome may as a result combine with some good genes in the other chromosome to create a better solution represented by the new chromosome. Figure 3 shows chromosome representation.

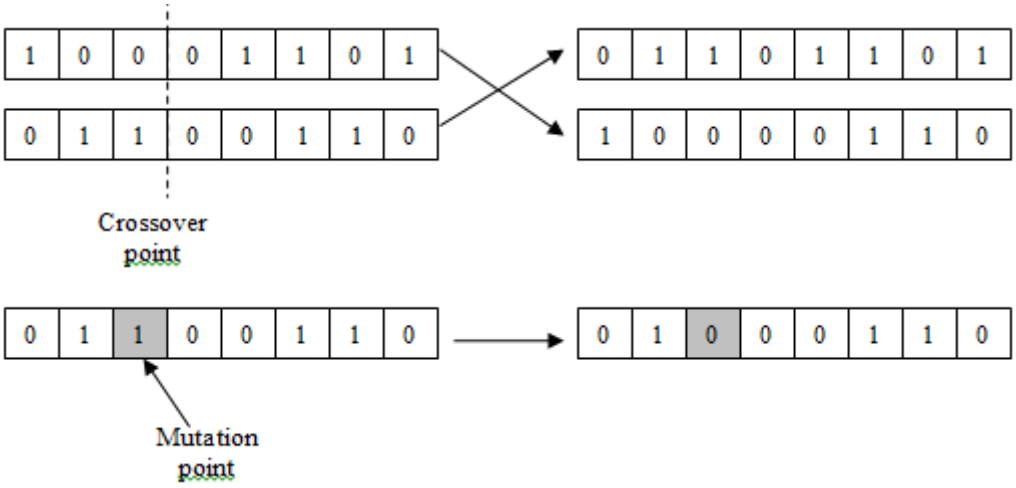

Figure 3. Chromosome representation

Mutation is a random adjustment in the genetic composition. It is useful for introducing new characteristics in a population – something not achieved through crossover alone. Crossover only rearranges existing characteristics to give new combinations. For example, if the first bit in every chromosome of a generation happens to be a 1, any new chromosome created through crossover will also have 1 as the first bit.

The mutation operator changes the current value of a gene to a different one. For bit string chromosome, this change amounts to flipping a 0 bit to a 1 or vice versa.

Although useful for introducing new traits in the solution pool, mutations can be counterproductive, and applied only infrequently and randomly

The steps in the typical genetic algorithm for finding a solution to a problem are listed below:

a. Create an initial solution population of a certain size randomly
b. Evaluate each solution in the current generation and assign it a fitness value.
c. Select "good" solutions based on fitness value and discard the rest.
d. If acceptable solution(s) found in the current generation or maximum number of generations is exceeded then stops.
e. Alter the solution population using crossover and mutation to create a new generation of solutions.
f. Go to step

4. IMPLEMENTATION FLOWCHART

Figure 4 shows flowchart of implemtation.

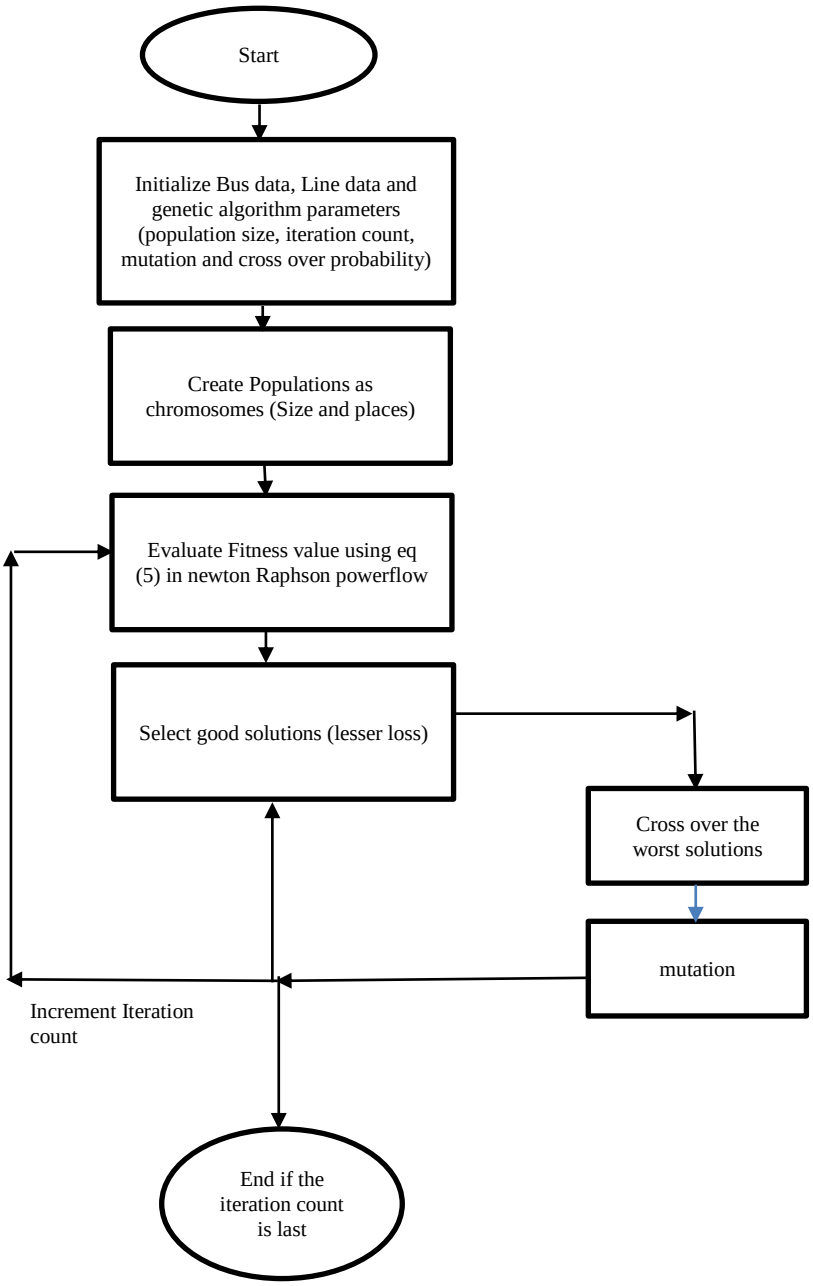

Figure 4. Flowchart of implemtation

5. RESULTS AND DISCUSSION

The IEEE 30 bus system is used to test the optimal sizing and placement of SVC concept. The system has 283.4 MW load of real power and 126.2 Mvar of reactive power with 100 MVA as Base power. Without SVC it produces 17.599 MW real power losses.

Figure 5 shows the before and after placement of SVC. The genetic algorithm is run for 500 iterations and 50 population (chromosomes). Identified best bus is 6th bus and the power SVC value placed is 1.3779 p.u of admittance. The power loss reduced to 6.2299 MW. The loss percentage improved is 64.6%.

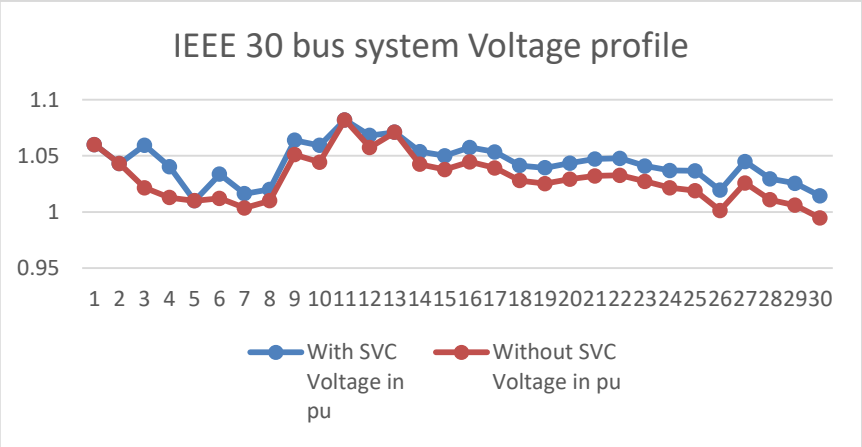

Figure 5. After and before placement of SVC

The voltage improvement indicates that the increase in loadability of the system. Figure 6 shows the voltage profile improvement in percentage and bar chart. Figure 7 shows the power factor improvement percentage in bar chart.

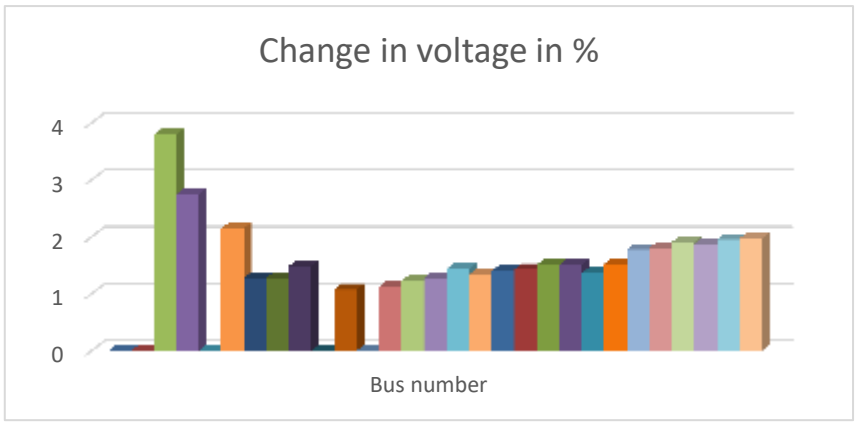

Figure 6. Voltage profile improvement in %

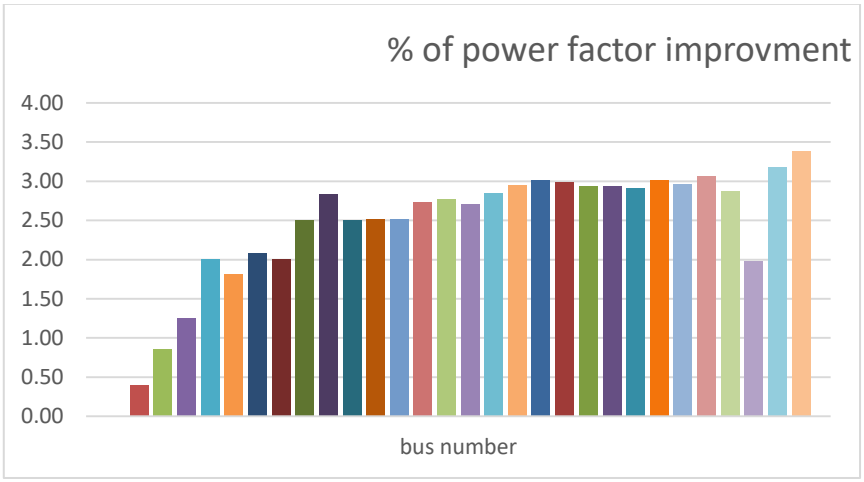

Figure 7. Percentage of power factor improvement in each bus

The Table 1 shows the with and without SVC placement. The Table 1 represents the voltage profile improvement in each bus after and before placing SVC. The 5th and 6th column indicates the power injection at each bus -ve symbol indicates load and +ve symbol indicated generation. The real power generation from slack bus is reduced due to the SVC placement and losses got reduced. The 7th and 8th column shows the power factor improvement after and before placement of SVC. last column shows the improvement of power factor after placing the SVC. At 30th bus the power factor improvement is high. From this results it can be concluded that a single SVC placement at 6th bus increases the loadability, reduces the losses and increases power factor and voltage profile. And it can be noted that placing at 6th bus not only effecting on 6th bus it improves the over all system performance.

Table 1. With and without SVC Placement Voltage, Power Injection and Power Factor

bus no.	With SVC Voltage in pu	Without SVC Voltage in pu	% increase in voltage	with SVC power injection	without svc power injection	with SVC power Factor	without SVC power Factor	% improve-ment power Factor
1	1.06	1.06	0.00	105.57	261.00	1.00	1.00	0.00
2	1.04	1.04	0.00	18.30	18.30	1.00	1.00	0.39
3	1.06	1.02	3.79	-2.40	-2.40	1.00	0.99	0.85
4	1.04	1.01	2.75	-7.60	-7.60	1.00	0.99	1.25
5	1.01	1.01	0.00	-94.20	-94.20	0.99	0.97	2.01
6	1.03	1.01	2.15	0.00	0.00	1.00	0.98	1.81
7	1.02	1.00	1.28	-22.80	-22.80	0.99	0.97	2.08
8	1.02	1.01	1.00	-30.00	-30.00	1.00	0.98	2.00
9	1.06	1.05	1.28	0.00	0.00	0.99	0.97	2.50
10	1.06	1.04	1.49	-5.80	-5.80	0.99	0.96	2.84
11	1.08	1.08	0.00	0.00	0.00	0.99	0.97	2.50
12	1.07	1.06	1.07	-11.20	-11.20	0.99	0.96	2.52
13	1.07	1.07	0.00	0.00	0.00	0.99	0.96	2.52
14	1.05	1.04	1.12	-6.20	-6.20	0.99	0.96	2.73
15	1.05	1.04	1.23	-8.20	-8.20	0.99	0.96	2.77
16	1.06	1.04	1.28	-3.50	-3.50	0.99	0.96	2.71
17	1.05	1.04	1.44	-9.00	-9.00	0.99	0.96	2.85
18	1.04	1.03	1.34	-3.20	-3.20	0.99	0.96	2.95
19	1.04	1.03	1.40	-9.50	-9.50	0.99	0.96	3.02
20	1.04	1.03	1.43	-2.20	-2.20	0.99	0.96	2.99
21	1.05	1.03	1.51	-17.50	-17.50	0.99	0.96	2.94
22	1.05	1.03	1.51	0.00	0.00	0.99	0.96	2.94
23	1.04	1.03	1.36	-3.20	-3.20	0.99	0.96	2.91
24	1.04	1.02	1.53	-8.70	-8.70	0.99	0.96	3.01
25	1.04	1.02	1.78	0.00	0.00	0.99	0.96	2.97
26	1.02	1.00	1.81	-3.50	-3.50	0.99	0.96	3.07
27	1.04	1.03	1.91	0.00	0.00	0.99	0.96	2.88
28	1.03	1.01	1.88	0.00	0.00	1.00	0.98	1.97
29	1.03	1.01	1.95	-2.40	-2.40	0.99	0.96	3.17

6. CONCLUSION

Optimal sizing and placing of SVC is implemented with genetic algorithm using IEEE 30 bus system. The system losses improved by 64.6% by using the loss function as objective function and place and size of SVC as chromosomes. by using 500 iterations and run the algorithm for multiple times we got best results as 6th bus and 1.3779 p.u as SVC admittance value. And it is identified that by reducing real power loss after placing SVC increases the overall voltage profile of the system and power factor of each bus nearly 0.99. Hence the performance of IEEE 30 bus system is improved by optimally placing the SVC with optimal size.

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