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FPGA Based Optimized Discontinuous SVPWM Algorithm for Three Phase VSI in AC Drives

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ABSTRACT

The discontinuous space vector pulse width modulation (SVPWM) has well-known that can reduce switching losses. By simplifying the thermal management issues, the discontinuous SVPWM can potentially reduce the inverter size and cost. However, using the modulation due to different time interval equations for each sector can introduce glitches at the points when the sector is changed. The more main problem, it can increase unwanted harmonic content and current ripple. Consider the decrease in switching losses associated with discontinuous modulation allows the system to utilize a higher switching frequency, this paper present high frequency switching of optimized discontinuous SVPWM based on FPGA to overcome the problems above. The proposed SVPWM has been successfully implemented by using APEX20KE Altera FPGA to drive on a three phase inverter system with 1.5 kW induction machine as load. The results have proved that the method can reduce harmonic content and current ripple without glitches.

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1. INTRODUCTION

The key requirements of any modulation method are to provide higher power output and efficiency for a wide range of inverter output voltage control. The SVPWM method is an advanced PWM method at which it is possibly the best among all the PWM techniques for variable frequency drive applications, since SVPWM can provide a better fundamental output voltage, better harmonic performance and easier be implemented [1-11].

The SVPWM strategies have been the focus of many years of research attempt. In recent years, the SVPWM method gradually obtains widespread applications in the power electronics and the electrical drives due to its superior performance characteristics. The SVPWM is more suitable for digital implementation compared to the SPWM, whereby the obtainable DC voltage utilization ratio can be highly increased. As the result, a better voltage THD factor can be obtained [1, 7, 9, 12-14].

The comparison of P_L, T_J junction IGBT, and weighted THD of the different modulation schemes are shown in Table 1 [15]. From the comparison, although the discontinuous SVPWM (or bus clamping SVPWM) gives a slightly higher of weighted THD compared with conventional SVPWM method, the result in lowest switching losses and lowest junction temperature of IGBT compared with the SPWM and conventional SVPWM. The switching loss of the discontinuous SVPWM is consistently lower than those of SPWM and SVPWM as there are fewer switching instants and that the dead-time effect is smaller since there is no switching during the DC clamped period.

Table 1. The comparison of the different modulation schemes [15]

Parameters	SPWM	Conventional SVPWM	Discontinuous SVPWM
P_L (per-unit of SPWM)	1.00	1.33	0.83
T_J (increase, °C)	35	45	32
Weighted THD (%)	4.0	1.8	2.9

At higher line-side voltages for a given average switching frequency, the discontinuous SVPWM have lower THD in line currents than the continuous SVPWM methods [2, 16-19]. The discontinuous SVPWM also provides a linear range of modulation index 0-115.4% [20]. It is, therefore, can increase the power handling capability of the converter, or its need for cooling, and increasing the converter power density. It is suitable to minimize the weight and volume of power electronics systems, as in electric vehicle and aircraft applications.

The discontinuous SVPWM initially developed by Depenbrock [21] in 1977. Currently, the discontinuous SVPWM has become one the most promising modern PWM methods which is used in various power electronics such as motor drives, front-end converter, and active filter. In general, it is now accepted that with discontinuous modulation having some advantages for higher modulation ratios [16, 22-28]. However, in the discontinuous SVPWM methods, the reduction in their switching loss does not exactly come free. There is a small drawback can introduce oscillations around the points where the sector is changed. This is due to the different set of equations used within each sector to calculate the time intervals. At low output fundamental frequencies, the effects will be clearer and they result in increased loss in the load and may cause instabilities of the feedback control system [5, 20, 29-31]. In this paper therefore the discontinuous SVPWM duty cycle is updated at specific times in the SVPWM period to avoid glitches in the PWM output signal.

The SVPWM algorithm is mainly implemented using software based on microcontroller or DSP [32-34]. Designers have to perform the control procedure sequentially by exploiting their mathematically oriented resources. That is the instructions of different procedures need to be executed one after the other. Thus, the purely software-based technique is not an ideal solution. The FPGA is an appropriate alternative over analog and software solutions (DSP and microcontroller) [35-39], and its architecture offers a significant integration density [40] within a flexible programmable environment. Designers can get a new degree of freedom by applying FPGA in SVPWM since their dedicated hardware architectures that match all the requirements in terms of control performance and implementation constraints can easily be realize [41].

Employing of FPGA in SVPWM methods offer a lot of advantages, such as: shorter design cycle, fair cost, rapid prototyping, simpler hardware and software design, and higher switching frequency. It is exactly different from software implementation, whereby the FPGA performs the entire procedures with concurrent operation (allow parallel processing by means of hardware mode and not occupying) by using its reconfigurable hardware. With the powerful computation ability and flexibility, an FPGA is quite mature for electrical drive application and it is considered as a solution to improve system performance of a digital controller, including a SVPWM algorithm [3, 41-47].

In many control applications, including SVPWM realization, the digital hardware FPGA-based solutions have been successfully used [3, 41, 43-46]. However, these conventional SVPWM suffers from the disadvantages like computational burden, low-grade performance at high modulation indices and high switching losses of the inverters. Therefore, several discontinuous SVPWM methods have been proposed to reduce the switching losses and to improve the performance in high modulation region [5, 13, 15, 16, 18-21, 26, 27, 48-55].

Although the researches of the implementation for three-phase SVPWM based on FPGA is not lacking, However, most of the designs are based on the conventional SVPWM without consideration of the hardware-resource saving and are more complex. In this paper, a new approach of FPGA-based SVPWM will discussed, where the judging of sectors and the calculation of the firing time to generate the SVPWM waveform is simple with low switching losses and hardware-resource saving. The quadrature voltages have be evaluated in time domain, as shown in Fig 1 to identify sector location. The proposed method is single stage comparator, so the identification will run quickly. As a result, the information of sector location will be informed only within one clock cycle to accurately select the voltage vectors. By using the relationship between carrier-based PWM and SVM, the calculating of the duration of active vectors will be represented in carrier based, so the calculation can be easily transformed in an equivalent space vector modulation modulator to generate SVM switching pulses. Therefore, it doesn't require for calculating the durations directly. The proposed SVPWM design will be implemented based on APEX20KE Altera FPGA.

2. NOVEL METHOD OF SVPWM ALGORITHM

The SVPWM strategy aims to minimize harmonic distortion in the current by selecting the appropriate switching vectors and determining of their corresponding dwelling widths. The choice of the null

vector determines the SVPWM scheme. There are some options: the null vector V0 only, the null vector V_7 only, or a combination of null vectors. The equivalent PWM waveforms, which produce the same average flux, may consist of various combinations of the basic vectors. The characteristic of each those strategies above can be resumed as shown in Table 2.

Table 2. Comparison of SVPWM patterns

No	Pattern SVPWM (based on sector I)	Number of segments	Number of commutation in one sampling period	THD	Easiness to implement in FPGA
1	V_0-V_1-V_2-V_7-V_2-V_1-V_0	7	6	low	quiet-difficult
2	V_7-V_2-V_1-V_0-V_1-V_2-V_7	7	6	low	quiet-difficult
3	**V_1-V_2-V_7-V_2-V_1**	**5**	**4**	**almost low**	**easy**
4	**V_0-V_1-V_2-V_1-V_0**	**5**	**4**	**almost low**	**easy**
5	V_0-V_1-V_2-V_7	4	3	almost significant	not-easy
6	V_0-V_2-V_1-V_7	4	3	almost significant	not-easy
7	V_1-V_2-V_7 and V_2-V_1-V_7 alternately	3	2 and 3 alternately	higher significant	not-easy

The conventional principle of the SVPWM algorithm relies too much on the judging of sectors, firing time (duration of active vectors) calculation, and the method of switching sequence generating are too complex. As a solution to overcome the problems from the conventional SVPWM, the paper proposes the principle of a symmetrical five-segment discontinuous switching sequence that not yet been revealed yet as a novel method of SVPWM algorithm.

2.1. Proposed SVPWM switching Pattern (five-segment discontinuous switching sequence)

It has been reported many discontinuous SVPWM patterns [3, 5, 52, 54, 56]. Unfortunately, these patterns performed with used a complicated algorithm and high switching losses that is not easily realized based on FPGA. This paper proposes a novel symmetric five-segment discontinuous SVPWM, the design of which mainly originated from the ideas of [33] and [57]. The pattern has been successfully DSP based implemented by Yu [33]. This pattern offered in lower switching losses, a simpler algorithm and easily implementation.

Therefore, in order to improve system performance, this paper will focus on implementation of discontinuous SVPWM pattern based on FPGA. There is always a leg that stays constant for the entire PWM period in this proposed pattern. The state sequence in this pattern is X-Y-Z-Y-X, where Z=1 in sector I, III and V, and Z=0 in the remaining sector. Thus, the number of switching time for this pattern is less than the conventional pattern, and the obvious result is reduced switching losses.

2.2. Proposed identification of the sector

Several methods have been introduced to judge the sector where the reference space voltage vector lies. Zhi-pu [58] compared the reference space vector's angle with 00, 60^0, 120^0, 180^0, 240^0, and 300^0 to achieve the number of the sector in which V_{ref} lies. Others, Yu [59], Jiang [60] and Xing [6] have analyzed the relationship between V_α and V_β to determine the sector.

They have calculated the projections V_a, V_b and V_c of V_α and V_β in (a,b,c) plane by using the inverse Clark transformation, as follow:

$$\begin{cases} V_a = V_\beta \\ V_b = \dfrac{\sqrt{3}V_\alpha - V_\beta}{2} \\ V_c = \dfrac{-\sqrt{3}V_\alpha - V_\beta}{2} \end{cases} \quad (1)$$

Then, based on equation (1) and Table 3, N=sign(Va) + 2*sign(Vb) + 4*sign(Vc) and map N to the actual sector of the output voltage reference by referring to the following relationship N➔sector: 1➔II, 2➔VI, 3➔I, 4➔IV, 5➔III, 6➔V. In [61], Zeliang et al. adopted two new intermediate vectors X_α and X_β whereby $X_\alpha = \frac{3}{2}V_\alpha$ and $X_\beta = \sqrt{3}V_\beta$.

Table 3. The proposed identification of the sectors

Sector	Vector Angle	$V_\beta > 0$	$V_\beta > \sqrt{3}V_\alpha$	$V_\beta > -\sqrt{3}V_\alpha$
I	(0^0, 60^0)	1	0	1
II	(60^0, 120^0)	1	1	1
III	(120^0, 180^0)	1	1	0
IV	(180^0, 240^0)	0	1	0
V	(240^0, 300^0)	0	0	0
VI	(300^0, 360^0)	0	0	1

1: satisfy, 0: not satisfy

Decomposing the conventional SVPWM will properly counteract the redundant calculations to identify sector location, but it result in complicated matrix calculations. In this paper, by analyzing on the principle of SVPWM in [6, 59-61] and to reduce burden of computation, a new method to determine the sectors of voltage vectors based on comparison between $V_\beta, \sqrt{3}V_\alpha, -\sqrt{3}V_\alpha$ and 0 as shown in Figure 1 is proposed. Through the comparison, sectors of voltage vectors as shown in Table 3 can be determined.

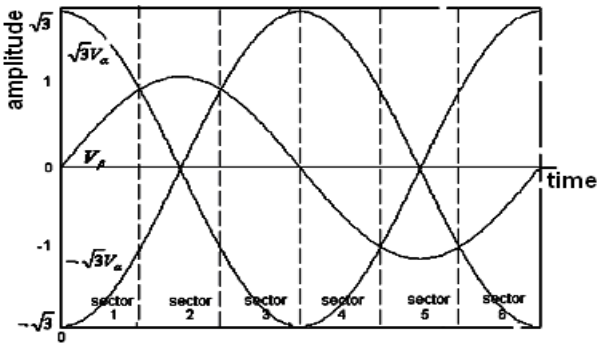


Figure 1. The plotting of $V_\beta, \sqrt{3}V_\alpha, -\sqrt{3}V_\alpha$ wave

2.3. The proposed calculation of the duration of active vectors

In this paper, a new set of equations to calculate the duration of active vectors for each sector has been re-arranged in order to construct an easier implementation based on FPGA. The space vector technique synthesizes a desired vector Vref from two adjacent actives, V_α and V_β (among V_1 and V_2, as shown in Fig.1) during time interval, T_a and T_b. The null vectors (V_0 and V_7) are also applied to reduce the inverter switching frequency. In the proposed design, only one null vector is inserted in a PWM period, whereby V_7 for odd sector and V_0 for even sector.

$$V_{ref} = V_\alpha + jV_\beta = \frac{2T_a}{T}V_\alpha + \frac{2T_b}{T} \quad (2)$$

$$\frac{T}{2} = T_a + T_b + T_0 \quad (3)$$

Hence, the half PWM period T is composed of the switching time Ta, Tb and T0. The total time of the null vectors can be expressed as

$$T_0 = \frac{T}{2} - T_a - T_b \quad (4)$$

In this design, the switching time of the active vectors for each sector can be calculated as shown in Table 4.

Table 4. Switching time of the active vector for each sector

Sector	T_a	T_b	T_a+T_b
I	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}+\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
II	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}+\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}+\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$
III	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}+\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
IV	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}+\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
V	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$
VI	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$

2.4. Proposed method to generate SVPWM switching pulses

In this paper, a new method to generate SVPWM switching pulses is proposed, whereby by using comparison between the triangle waveform with T_a and T_a+T_b, the PWM signals for odd sectors are realized. High signal will be generate when the triangle waveform is higher than signal A or B, and another leg is always set to 1. While for the even sectors, the generation of PWM signal is complement with the odd sectors. Whereby signal will set high when the triangle waveform is lower than signal A or B and another one leg is set to 0.

To simplify the design process, the term $\frac{2m}{T}$ will set to 1so that y will be always equal to x (x=$T_0/2$ =Ta then y=x=Ta, and if x=$T_1/2$ then y=$T_1/2=T_b$). Obviously if x=$\frac{T_0}{2}+\frac{T_1}{2}=T_a+T_b$ then y=$\frac{T_0}{2}+\frac{T_1}{2}=T_a+T_b$. Therefore, the generation of PWM for S_b and S_c legs in sector I can be obtained by comparing the triangle waveform with T_a, and T_a+T_b respectively and $_{Sa}$ Leg is set to 1 due the odd sector position as shown in Figure 2.

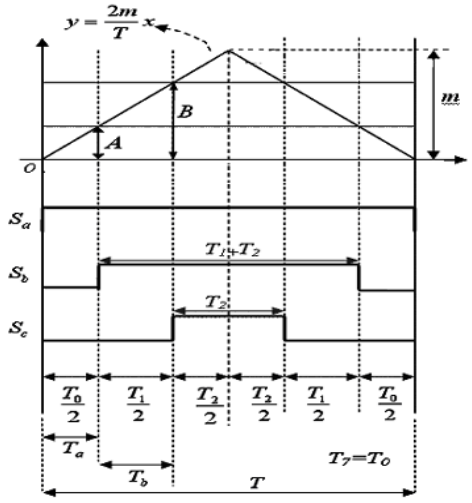


Figure 2. Proposed SVPWM switching sequence generating method

3. FPGA IMPLEMENTATION OF A PROPOSED NOVEL SVPWM

After the principle of SVPWM generation is discussed above, this section will focus on implementation of FPGA in SVPWM. To simplify the implementation based on FPGA, a graphical method has been devised to generate the SVPWM switching pulses. The overall proposed SVPWM design is shown in Figure 3. From this Fig, it consists of 6 blocks or modules, namely *ajust_freq*, *Vbeta_Valfa*, *find_sector*, *SVPWM_generator, fw-rv* and *deadtime_sytem* modules. Each module is explained as follow:

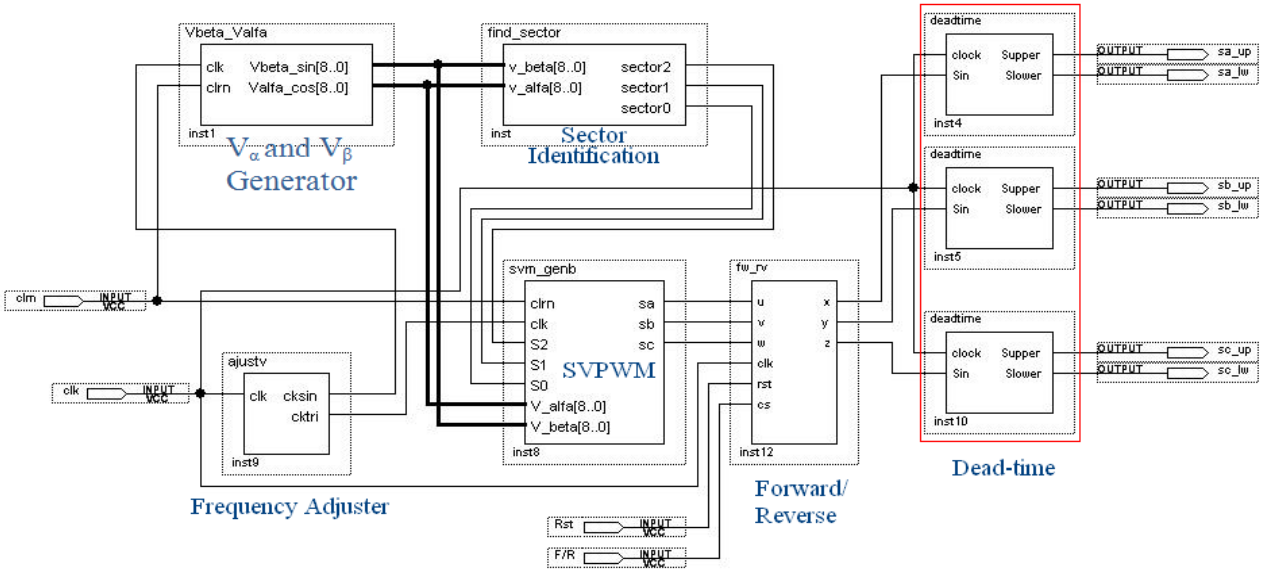


Figure 3. The prototype of the proposed SVPWM design

3.1. First Module: "ajust_freq"

From Figure 3, the function of ajust_freq is to generate a suitable clocking frequency. In the proposed SVPWM design, this module functions as a frequency divider by generating a carrier frequency of 20 kHz and a fundamental frequency of 50 Hz from the FPGA board, which have a clocking signal of 33.33Mhz. Since the triangle signal generator in this design is sampled to be 32 times per period, in order to get a carrier frequency of 20kHz, the main clock generator from FPGA board (pin L6)was divided by 13 (33.33MHz:(13 x32) =20kHz). The reference signal clocking is produced in a similar way.

3.2. Second Module: "Vbeta_Valfa"

In the proposed method, V_{alfa} and V_{beta} are generated based on sine and cosine functions through the look up table (LUT) with memory mapping. There have three lines which categories as lower, base and upper that represented to avoid overflow. With the memory mapping of 360 addresses, the counter mod-360 will used to count LUT of V_{alfa} and V_{beta}. In a similar way, the expansion of the module can be easily implemented. However, the using two's complement fixed-point format is more suggested compared to unsigned format as used in the prototype.

3.3. Third Module: "find_sector"

A reference voltage sector is necessary due to the different of switching time equations. The sector finder (SF) module in this design is used to judge the reference vector sector by referring to Table 3, is shown in Figure 4. This module determines the number of sectors and simplifies the truth table by comparing the above-mentioned results.

3.4. Fourth Module: "SVPWM_generator"

This module was divided into 4 sub modules, namely Triangle, Duration_Ta, Duration_TaTb, and SVPWM pattern module. Triangle module is functioned as triangle signal generator. The Duration_Ta and Duration_TaTb module are digital solutions for each second and fourth column, respectively. Finally, the SVPWM pattern module is used to generate the SVPWM sequence as described in section 2.4.

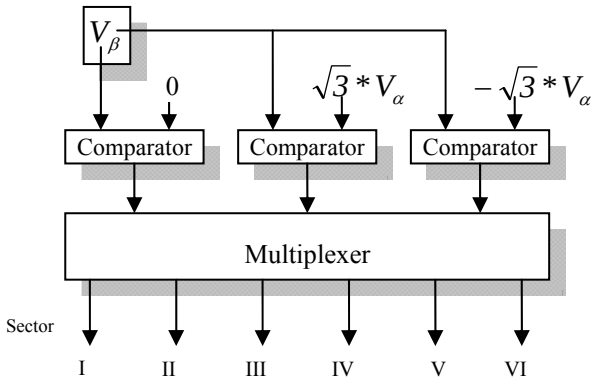


Figure 4. The proposed section determination

If it is assumed that T/VDC=1 and consider Figure 2 and Table 4, then the duration determination of Ta and Ta+Tb, and SVPWM pattern (switching status of Sa, Sb and Sc) can be calculated as shown in Table 5.

Table 5. The duration determination of T_a and $T_a + T_b$, and SVPWM pattern (switching status of S_a, S_b and S_c)

Sector	T_a	T_a+T_b	S_a	S_b	S_c
I	V_d - 0.577V_q	V_d + 0.577V_q	1	Tri CP T_a	Tri CP T_a+T_b
II	V_d + 0.577V_q	+ 1.732V_q	not (Tri) CP T_a	not (Tri) CP T_a+T_b	0
III	1.155V_q	-V_d	Tri CP -(T_a+T_b)	1	Tri CP T_a
IV	-V_d + 0.577V_q	-V_d - 0.577V_q	0	not (Tri) CP T_a	not (Tri) CP T_a+T_b
V	-V_d - 0.577V_q	- 1.732V_q	Tri CP T_a	Tri CP T_a+T_b	1
VI	- 1.155V_q	V_d - 0.577V_q	not (Tri) CP T_a+T_b	0	not (Tri) CP T_a

Tri: triangle signal; CP: compared to, "1" if equal or higher and "0" if lower; Not: NOT operation

3.5. Fifth Module: "fw_rv"

By including this module, we are possible to control forward and reverse motor direction. In this design, cs is used to change one of the forward or reverse control.

3.6. Sixth Module: "deadtime_system"

A dead-time of at least 2 μs is required to avoid short circuit within a leg. Pair of 16-bits counter and 16 bits comparator is used to construct the dead time generator for each leg.

4. RESULTS AND DISCUSSIONS

The software to design, perform compilation, verification and develop hardware based on the APEX20KE FPGA was developed under the Altera Quartus II, version 9.0. When compared with others methods, the proposed method required the minimum hardware resources. Tzou [3], Moreira [42], Zhaoyong [43], Guijie [47] and [56] consumed 2880, 1156, 3011, 1159, 3011 LEs respectively. The proposed SVPWM only consumed 520 LEs.

Figure 5 show output of the FPGA-based proposed discontinuous SVPWM generator which are acquired by Zeroplus Logic cube LAP-C 16064 logic analyzer. The photograph of the hardware experimental setup is shown on Figure 6.

In this paper, the proposed SVPWM generator design with different carrier frequencies were successfully been carried out using of APEX20KE Altera FPGA. The results from hardware implementation with this proposed SVPWM generating method at carrier frequency of 20 kHz is shown in Figure 7. Probes 1, 2 and 3 in Figure 7 (a) and (b) represent switching state of S_a, S_b, and S_c, respectively, whereby the probe M is a (S_a+S_b) line-to-line switching state with its frequency spectrum. From Figure 7 (b), the harmonics due to the 20 kHz switching frequency are clearly visible.

The similar condition is shown in Fig. 8. In this case, carrier frequency is set to 40 kHz, although the result in Fig. 8 (b) shows a 40 kHz. To test on the performance for the proposed SVPWM generator based

FPGA design, a three phase inverter system together with an induction machine of 1.5 kW is used.

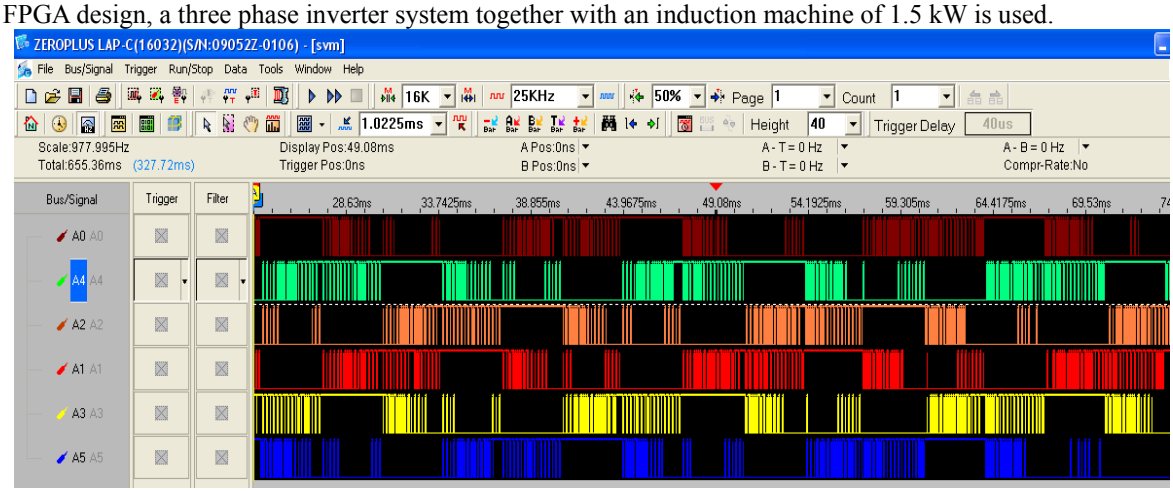


Figure 5. The comparison of required hardware resources

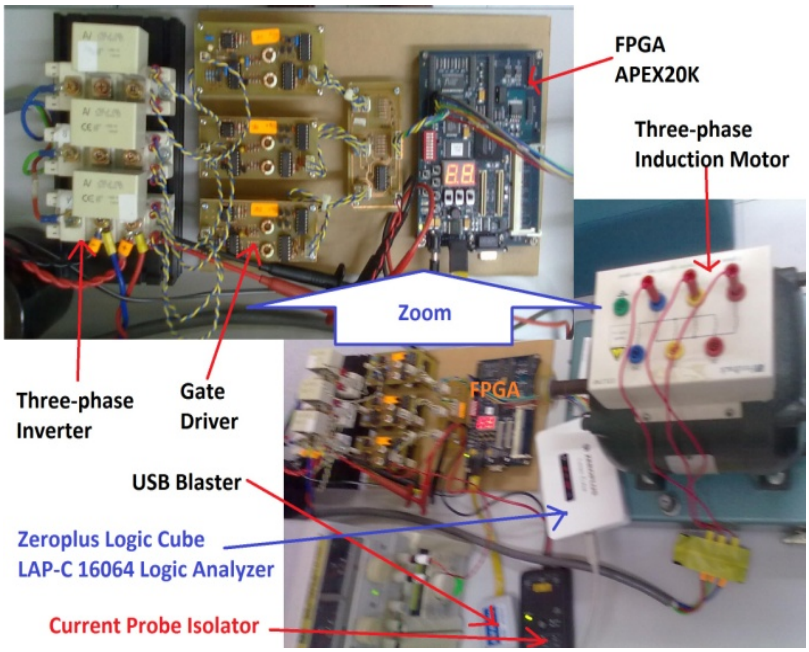
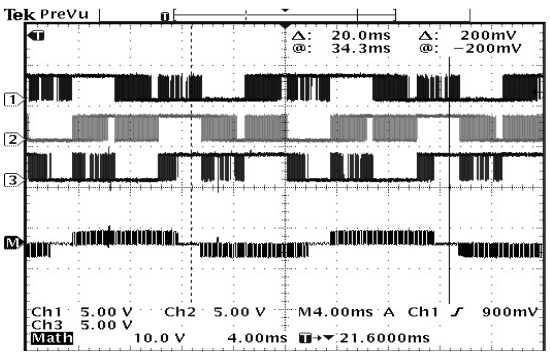
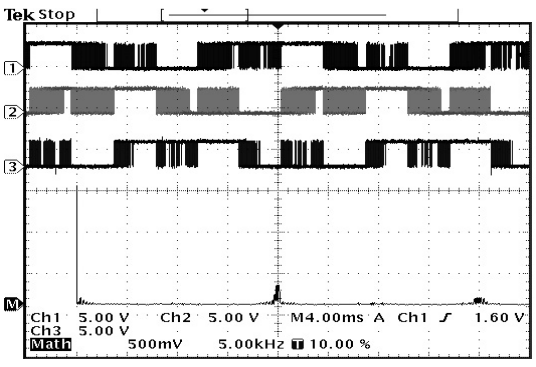


Figure 6. The hardware experimental setup

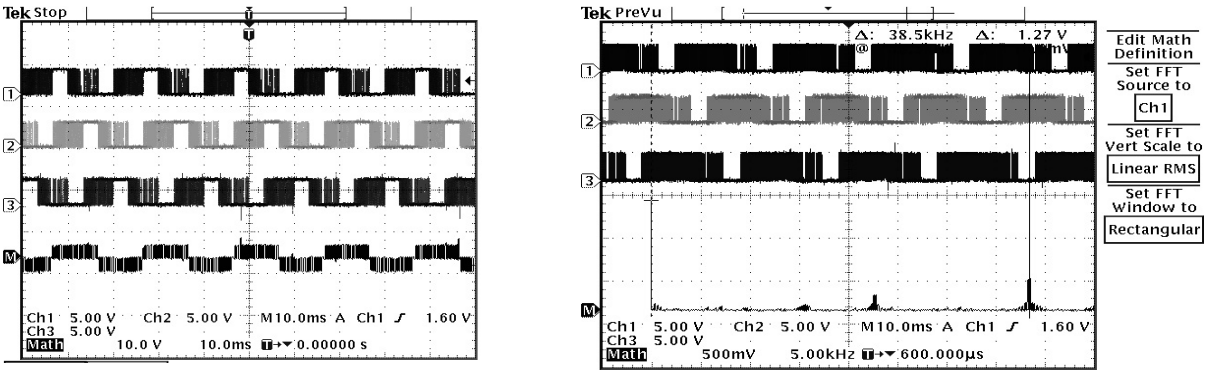


(a) the switching state and its line-to-line



(b) The signal gating and its frequency spectrum

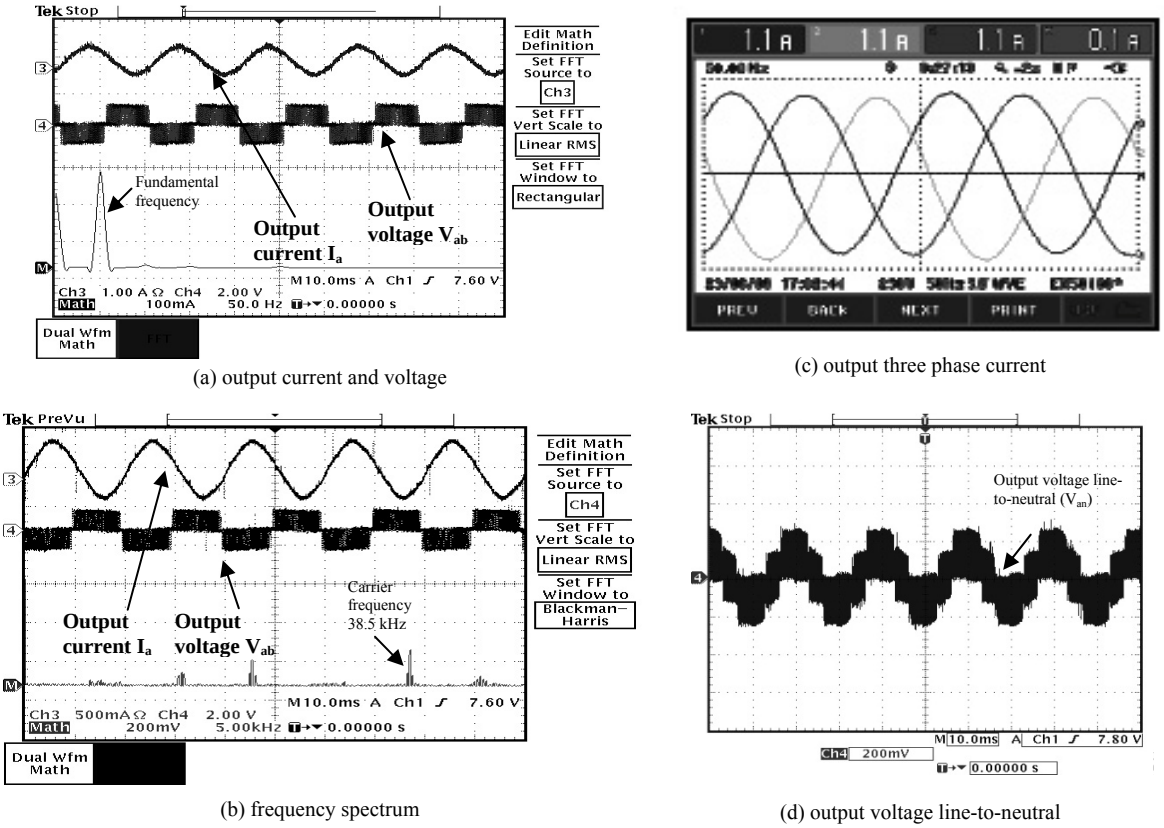
Figure 7. Hardware implementation of proposed SVPWM generator at carrier frequency 20 kHz.



(a) the switching signals and line-to-line switching

(b) The signal gating and its frequency spectrum

Figure 8. Hardware implementation of proposed SVPWM generator at carrier frequency 40 kHz.



(a) output current and voltage

(c) output three phase current

(b) frequency spectrum

(d) output voltage line-to-neutral

Figure 9. The performance of FPGA based proposed SVPWM generator design

The practical result for output stator current (I_a), output phase-to-phase voltage (V_{ab}), frequency spectrum, output three phase current and output voltage line-to-neutral (V_{an}) are shown in Fig. 9. The results shows that this proposed-SVPWM-generator based FPGA design is successful when implemented through a hardware platform. The practical results from the test-rig were as expected and showed that the proposed SVPWM generator design has successfully driven a 1.5 kW induction machine, with low current ripple. The result is in-line with [16] and [22] that the RMS current ripple at higher modulation indexes can be significantly reduced by using the discontinuous SVPWM.

Further, the comparison of current and voltage THD between the proposed SVPWM and other SVPWM is shown in Table 6. From the table, the proposed SVPWM shows a lower percentage in current and voltage THD compared with other SVPWM. However, the current THD from the proposed SVPWM (6.4%) is slightly higher than the hybrid type IV that proposed by Zhao *et al* [40] which is 6.34%. In addition, the

voltage THD is 11.10% and is slightly higher than the pattern III that proposed by Bharatiraja et al [56] with 9.90%.

Table 6. Comparison of current and voltage THD between the proposed SVPWM and other SVPWM

Strategy	Current THD (%)	Voltage THD (%)	Fundamental frequency (Hz)
Proposed SVPWM based on FPGA	**6.40**	**11.10**	50
Zhang and Yu [52]			
- 3-segment SVPWM	not reported	69.38	50
- five-segment SVPWM	not reported	68.52	50
- 7-segment SVPWM	not reported	66.59	50
Narayanan et al [53]			
- Conventional SVPWM	20.29	not reported	60
- Discontinuous SVPWM	15.37	not reported	60
- Three-zone hybrid PWM	13.00	not reported	60
- Five-zone hybrid PWM	12.72	not reported	60
- Seven-zone hybrid PWM	12.58	not reported	60
Bharatiraja et al [56]			
- pattern I	15.07	17.60	50
- pattern II	19.31	**9.90**	50
- pattern III	23.96	24.27	50
Saad et al [62]			
- Rising-edge aligned sequence scheme (SVPWM1)	not reported not reported	54.49 54.47	not reported not reported
- Falling-edge aligned sequence scheme (SVPWM2)	not reported not reported	54.45 39.86	not reported not reported
- Symmetric aligned sequence scheme (SVPWM3)			
- Alternative sequence scheme (SVPWM4)			
Zhao et al [63]			
- Conventional SVPWM	10.07	not reported	50
- Minimum switching loss PWM (MSLPWM)	10.11	not reported	50
- Discontinuous SVPWM	7.64	not reported	50
- Hybrid Type I	6.43	not reported	50
- Hybrid Type IV	**6.34**	not reported	50

5. CONCLUSION

This paper has proposed an advanced discontinuous (bus clamping) space vector modulation which employ special switching sequences and its implement special technique in FPGA hardware to get higher performance in term both in line current distortion as well as inverter switching losses, and also both in term of the hardware resources saving and the ease of implementing. The pattern is symmetrical will not degrade the control performance. The center-pulse switching pattern results will allow reducing the commutation losses and/or the harmonic content of output voltage, and to obtain higher amplitude modulation indexes if compared with conventional SVM. We have transformed the calculating of the duration of active vectors into an equivalent space vector modulation modulator to generate SVM switching pulses such as carrier-based PWM, so the calculation can be easily and fastly implemented in FPGA. The proposed SVPWM scheme has been successfully designed and implemented through the APEX20KE Altera FPGA in valuable hardware resources saving, without computing the number and angles of each sector as well as the commutation pattern. The practical results from the test-rig with a carrier frequency up to 40 kHz were as expected and showed that the proposed SVPWM generator design has successfully driven a 1.5 kW induction machine, with low current ripple and lower percentage in current and voltage THD compared with other SVPWM.

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