Application of Distribution Power Electronic Transformer for Medium Voltage

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ABSTRACT

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In this paper a distribution power electronic transformer (DPET) for feeding critical loads is presented. The PE based transformer is a multi-port converter that can connect to medium voltage levels on the primary side. Bidirectional power flow is provided to the each module. The presented structure consists of three stages: an input stage, an isolation stage, and an output stage. The input current is sinusoidal, and it converts the high AC input voltage to low DC voltages. The isolated DC/DC converters are then connected to the DC links and provide galvanic isolation between the HV and LV sides. Finally, a three-phase inverter generates the AC output with the desired amplitude and frequency. The proposed DPET is extremely modular and can be extended for different voltage and power levels. It performs typical functions and has advantages such as power factor correction, elimination of voltage sag and swell, and reduction of voltage flicker in load side. Also in comparison to conventional transformers, it has lower weight, lower volume and eliminates necessity for toxic dielectric coolants the DPET performance is verified in MATLAB simulation.

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1. INTRODUCTION

Distribution power Electronic Transformer (DPET) is a new type of transformer, which realizes voltage transformation and performs power quality functions through modern power electronic converters. In fact, DPET provides a fundamentally different and more complete approach in transformer design by using power electronics on the primary and secondary sides of the transformer. With the aid of multilevel converters on the line side, a high voltage interface with the utility Alternating Current (AC) system is provided, meanwhile with the aid of high performance3 phase inverter on the load side, a low voltage interface with consumer applications is produced. These new type of transformers have been introduced to eliminate the drawbacks of conventional copper- and-iron based transformers [1]-[6]. Those heavy and bulky transformers are fundamental components in power distribution systems. They are relatively inexpensive, highly reliable, and fairly efficient.

However, they have some disadvantages such as heavy weight, sensitivity to harmonics, voltage drop under load, (required) protection from system disruptions and overload, protection of system from problems arising at or beyond the transformer, environmental concerns regarding mineral oil, and lowperformance under dc-offset load unbalance. These disadvantages are becoming increasingly important as power quality becomes more of a concern [1]. For realization of PET, different topologies in literature have been presented [1]-[6]. Reference [2] applies an AC/AC buck converter to reduce input voltage to a lower one. In this structure for working at medium voltage levels, it needs a lot of series tied power

switches, which are difficult to control and stress factor would be high. Also the structure suffers lack of magnetic isolation and doesn't perform power factor correction. Considering above points, the AC/AC buck converter is not practical for medium voltage applications [1]. Another approach to realize DPET structure has been introduced in [3]-[4]. They use the concept of a high-frequency AC/AC link, termed as electronic transformer. Inthis Approach; the line side AC waveform is modulated to a high frequency square wave and passed through a HF transformer and again with a synchronous converter, it is demodulated to AC form. This method solves the lack of magnetic isolation but yet it doesn't perform power factor correction or is not applicable for high voltage applications. Reference [1] and [5] propose a structure based on input series output-parallel connection of converters to realize DPET structure. Those schemes are extremely modular and perform power quality functions. However they use high frequency switching, so they have low efficiency. Also all the series converters should work simultaneously which this fact reduces the availability and reliability of the system.

In [6] a new topology based on back-to-back diode- clamp multilevel converter has been introduced. It performs different power quality functions and prepares magnetic isolation. However for high voltage applications, it has a limitation on the number of voltage levels. Because, by increasing the voltage levels beyond five or six, the practical problems such as packaging problems and physical layout difficulties appear.

This paper presents a new topology of DPET based on multilevel converter. For balancing DC buses, a new and simple control method has been presented. In comparison with [1] and [5], it has better efficiency and its reliability has been improved. The structure is extremely modular and there is no limitation for voltage levels. The proposed DPET performs power quality functions beside the voltage reduction. It corrects the input Power factor, regulates the load voltage, and acts such as VAR compensator. It can also greatly alleviate the power quality susceptibility of the distribution level transformers on both source and load sides.

2. SYSTEM CONFIGURATION

A new DPET topology is proposed. As shown in Figure 1, it is constructed based on modules and a common dc link, which is used to transfer energy between ports and isolate all ports from each other. In this bidirectional topology, each port can be considered as an input or output. Each module consists of three main parts, including modulator, demodulator, and high frequency isolation transformer (HFIT). The modulator is a DC/AC converter and the demodulator is an AC/AC converter; both with bidirectional power flow capability. Each module operates independently and can transfer power between ports. These ports can have many different characteristics, such as voltage level, frequency, phase angle, and waveform. As a result, PET can satisfy almost any kind of application, which are desired in power electronic conversion systems and meet future needs of electricity networks.



Figure 1. Proposed DPET

In this paper, a modular structure based on the classification system given in [11] is proposed (Figure 2). The main AC/DC converter is placed in switch shown in Figure 2 is composed of "N" Half-bridge (HB) cells connected in series on the primary side and "N" DC/DC converters connected in series on the secondary side. The DPET structure can also be rearranged to supply different types of electric loads simultaneously.



Figure 2. DPET schematic diagram

This capability is shown in Figure 2 where 3 series- output cells will supply a three-phase voltage source inverter and the remaining cells will supply individual loads. In this case, the input power fed to the series Half-bridges in switch would be different. Therefore, the HB rectifier should maintain voltage balance among the primary DC links and correct the input power factor. Another challenging issue is related to the equal load-current sharing among the series cells. A very small mismatch among the series cells can cause a large current deviation among them. This problem, in practice, is intensified by the non-ideality of series cells.

2.1. Input Stage Power

The input stage is a multilevel HB rectifier, which is particularly attractive in high voltage applications. This structure is extremely modular, it has a simple physical layout, and it needs the lowest number of components in comparison with other multilevel converters. This paper focuses only on the single-phase HB rectifier. The three-phase structure is obtained by association of three Single-phase HB converters connected in a star configuration. Furthermore, bidirectional power flow can be realized from the bidirectional rectifier by turning off the top switches in all Half-bridges. In this work, a single-phase bidirectional HB converter is analyzed, and the results can be used either in a bidirectional converter or a three-phase system. In Figure 2, there are "N" series-connected Half-bridge cells and each cell can generate three voltage levels on the AC side: $0, +V_C$ and $-V_C$, where V_C is the desired DC-link voltage. Thus, using "N" Half-bridge cells, a maximum of 2N+1 different voltage levels are obtained to synthesize V_{an} or V_1 (AC terminal voltage):

$$V_{in} = \sum_{i=1}^{N} V_{hi} \tag{1}$$

$$V_{hi} = h_i V_{ci}, i = 1, 2... N$$
 (2)

Where V_{hi} , V_{Ci} and hi are the AC terminal voltage, the capacitor voltage and the switching function of ith Half-bridge, respectively. Applying Kirchhoff's voltage law (KVL) at the input voltage loop yields:

$$V_{in} = V_{an} + L_b(dl_{in}/dt)$$
(3)

Where Vin is the input voltage, Iin is the input current, and Lb is the input inductance which is used to shape the input current. Applying Kirchhoff's current law (KCL) for each cell leads to:

$$\mathbf{I}_{\mathrm{hi}} = \mathbf{h}_{\mathrm{i}} \mathbf{I}_{\mathrm{in}}, \, \mathbf{i} = 1, \dots, \, \mathbf{N} \tag{4}$$

Where I_{hi} is the output current of ith Half-bridge and is a function of the input current. Equation (1)–(4) describe a linear time varying (LTV) system with one input (Vin) and N+ 1 states (V_{C1} to V_{CN} and I_{in}). The HB controller should determine the switching functions, h_1 to h_N , in order to achieve the control goals.

2.2. Isolation Stage

The second part of the DPET structure (Figure 2) contains the isolated DC/DC converters. These converters are connected to the HB converter links and provide a highly stable DC interface on the LV side. In the above topology, several isolated converters can be series on the LV side to increase the power

capacity. However, the series cells should share the load-current equally and uniformly, in order to achieve identical operating conditions. This fact is also important from a thermal viewpoint.

In the isolation stage, different kinds of DC/DC converters can be utilized. Nevertheless, we use a bridge converter, which is the best in terms of efficiency and voltage stress. Among the bridge topologies, the zero voltage switched converter has a better performance than alternative topologies. All switches, in this topology, are turned on in the ZVS condition, and the turnoff losses are controlled by the series capacitors. Furthermore, in this DPET application, we need good voltage isolation between the HV and LV sides, which corresponds to high leakage inductance. Therefore it appears more reasonable to use a zero voltage switched converter as opposed to other alternatives that require a low leakage inductance transformer.

2.3. Output Stage

The output stage usually contains a single-phase or three-phase voltage source inverter that is connected to the DC bus and generates the AC output with the desired amplitude and frequency. The DC bus may also connect directly to a DC load or to a combination of AC and DC loads.

3. CONTROL STRATEGY FOR PET

Among multilevel converters, the bridge topology seems particularly attractive in high voltage applications. The major drawback of the topology is its requirement to isolated DC sources when it is used as an inverter. Notwithstanding, whenever it is used as an active rectifier, the topology is even more attractive because of the available distinct DC links feeding different loads. However in rectification mode there is possibility of instability in balancing of DC buses, and consequently the collapsing of switches and converter. Another parameter which should be considered, in study of rectifiers, relates to power factor correction capability and the reduction of input harmonics.

In literature various control methods for solving the instability problem of DC buses have been proposed. Unfortunately most of these methods have been limited to two series Half-bridges because of the control complexities, but in this paper a novel and simple method for controlling n half -bridges has been proposed. The proposed method guarantees the voltage balancing of DC buses even though the unequal loads have been connected to distinct DC buses. In addition it programs the input current to be in sinusoidal form, in phase or other phase angles with the input voltage.

In Figure 3(a), the control block diagram of HB rectifier has been shown. It contains two main parts: analog controller and software section. The analog controller prepares the vital Q signal for software section. Then the software section will define the best switching commands for Half-bridges.

In Figure 3(b), the detail scheme of analog controller has been shown. It contains a PI controller for regulating the total voltage of distinct DC buses to the desired reference value of nV_c . Next, the output of PI controller is multiplied by the mains voltage waveform to generate the desired reference of input current. Since the mains voltage is sinusoidal, the reference value of input current is also sinusoidal. For specifying the phase angle between input voltage and current, a time delay is used between input voltage and multiplier. Without it, the input current and voltage would be in phase.



Figure 3(a). Control block diagram

Figure 3(b). Analog controller used in Figure 3(a)

A hysteresis current comparator is employed in the inner control loop. It programs the input current to be in sinusoidal form and in phase with the mains voltage. This comparator generates the Q signal for the software section. This signal has the following meaning:

Q=0, Iin* +h<Iin

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$$Q=1$$
, $Iin < Iin^* -h$

(5)

Where, h defines the hysteresis band of current controller. If the line current increases from upper hysteresis band, Q will be zero to indicate the current reduction command. And if the line current decreases from lower hysteresis band, Q will be one to specify the current increase command.Before defining the control rules, the meaning of voltage regions should be defined. In fact, the input voltage is divided to n regions and each region is defined as following:

Region k:
$$(k-1)V_{C} < |V_{in}| kV_{c} < 0 \le k \le n$$
 (6)

Where, V_C is the desired value of DC capacitors insteady state and k is a nonnegative integer number. In Figure 4, voltage regions of input voltage have been shown. As it can be seen, in each region the AC terminal voltage of rectifier (V_{an}), can take only two values (k-1) V_C or kV_C . For specifying the proper value of Van, the software algorithm uses these rules:

- a) If $V_{in} > 0$ and $I_{in} > 0$ and Q=1 then $V_{an} = (k-1)V_c$ else if $V_{in} > 0$ and $I_{in} > 0$ and Q = 0 then $V_{an} = kV_c$ and zor balancing DC buses, capacitors with lower voltages are chosen to be charged.
- b) If $V_{in} > 0$ and $I_{in} < 0$ and Q=1 then $Van = (k 1)V_c$ else if $V_{in} > 0$ and $I_{in} < 0$ and Q = 0 then $V_{an} = kV_c$ and for balancing DC buses, capacitors with lower voltages are chosen to be charged.
- c) If $V_{in} < 0$ and $I_{in} > 0$ and Q=1 then $V_{an} = -kV_c$ else if $V_{in} < 0$ and $I_{in} > 0$ and Q = 0 then $V_{an} = -(k-1)V_c$ for balancing DC buses, capacitors with lower voltages are chosen to be charged.
- d) If $V_{in} < 0$ and $I_{in} < 0$ and Q=1 then $V_{an} = -kV_c$ else if $V_{in} < 0$ and Iin < 0 and Q = 0 then $V_{an} = -(k-1)V_c$ and for balancing DC buses, capacitors with lower voltages are chosen to be charged.



Figure 4. Identifying voltage regions for input voltage

For instance, in rule one when the input voltage and input current signals are positive and voltageregion is k, the value of V_{an} will be (k-1) V_C if Q=1 and k V_C if Q=0 for increasing or decreasing the input current as following:

$$Q=1: \Delta i + = +(V_{in}-(k-1)V_c) t_{on} / L_b$$

$$Q=1: \Delta i + = -(kV_c - V_{in}) t_{off} / L_b$$
(7)

Where, L_b is the boost inductor used for shaping the input current. To be noticed that this inductor will not see voltage more than $\pm V_c$. In addition in rule one, for synthesizing Van, those capacitors with lower voltages are chosen to be charged by positive current, meanwhile the total voltage of capacitors will be regulated by a PI controller to the reference value of nVC.If the rectifier application is limited to unity powerfactor applications, then the rules two and three are omitted and the power structure will be such as one shown in Figure 2. Second stage of DPET is the isolation stage which contains n isolated half bridge DC/DC converters connected to distinct DC links. In primary, the converters are arranged in series connection to provide the task of voltage reduction but in load side they are series to make common DC link. Here there ispossibility for working such as interleaved converters. For achieving this goal, those half-bridge converters have equal duty cycles and the gate signals are phase shifted equal to T_s/n (T_s defines the switching period of converters). By applying this technique, the output current ripple reduces considerably and efficiency increases. In Figure 5, the common DC link current (I_L+i_C) for two cases (before and after using the interleaving method) has been shown. It can be seen, by applying the interleaving technique, the current ripple reduces significantly.

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Finally by connecting the three phase voltage source inverter to common DC bus, the DPET structure is completed. In this paper, the voltage source inverter is controlled by PWM method. In this case, the direct axis, quadratic axis, and zero sequence quantities for three-phase sinusoidal signal is computed by transformation. Then the dq voltage terms are compared by reference signals $V_{dre}f=1$ and $V_{qref}=0$ and error signals enter to PI controllers. Then the PI outputs transformed to three-phase sinusoidal abc voltage terms and are used to generate appropriate inverter gate pulses.



Figure 5. Common DC link current before and after using the interleaving

4. RESULTS AND ANALYSIS

4.1. Simulation Result

The configuration which has been chosen to confirm the controller behavior is a converter with 5 Half-bridges. The RMS value of input Phase-Phase voltage is 3.3kV, so the nominal peak voltage of each phase will be 2694V. The reference value of DC buses is 600V, and nominal power of each Half-bridge is chosen to be 6kW, so the nominal power of rectifier will be 30 kW. The hysteresis band of input current and voltage ripple of capacitors have been set to ± 1 Ampere and ± 40 volt, respectively. According to above assumptions, the inductor and capacitors value arecalculated as 4mH and 60μ F. First simulation shows the general behavior of bridge rectifier while its Half-bridge outputs have been connected to different resistor loads (in Figure 2, consider resistor loads instead of half-bridge converters). In Figure 6, the Half-bridge DC buses waveforms have been shown. As can be seen, in spite of different load values, DC buses are well approached to reference value of 600V. This result confirms the appropriate voltage balancing of capacitors.



Figure 6. Voltage waveform of DC buses

In Figure 7, the line current has been shown. As can be seen, the input current amplitude has increased from 10A to 25.2A during load variation period. This is logical because the controller should increase the input current proportional to the load demand. For investigation about the power factor correction ability, the input current and input voltage waveforms have been shown together in Figure 7. It is obvious that the signals are in phase (PF=1) and current shape is sinusoidal. Also the THD of input current is 12% and it is compatible with IEEE 519-1992 standard. To be noticed that by increasing the load current, the input current distortion will decrease more.



In Figure 8, the total AC terminal voltage of rectifier (V_{an}) and individual AC terminal voltage of half bridges have been shown, respectively. This waveform is obtained by summing the individual AC terminal of H-bridges. Investigation of bottom waveform reveals the good switching characteristics for half bridges, because the number of switching transitions is lower than 30 and a good efficiency can be obtained.



Figure 8. AC terminal voltage

For simulation of PET, we use the structure shown in Figure 2. The bridge rectifier is same as the one stated in previous section. The parameter and component values used in simulation have been listed in appendix.1. In first simulation, the PET response to voltage sag condition is considered. In this case, the load power is 30 kWandinput voltage amplitude decreases 50% betweent=1.2sandt=1.4s. The simulation result for this case has been shown in Figure 9. As it can be seen, inspite of heavy voltage deep, the load voltage (phase- neutral voltage) iswell regulated and only in transient points there are small and short voltage variations.



Figure 9. Input voltage in SAG and SWELL

Second simulation investigates the PET response to voltage swell conditiont that is indiactaed by black mark cicle In this simulation the load power is 30kW and input voltage amplitude increases30% between t=1s and t=1.2s. The result for this case has been shown in Figure 9. It can be seen despite the voltage swell; again the load voltage is well regulated.

For achieving this goal, the controller increases the reference value of DC buses to V_C = 600V (upper limit). Figure 10 show that 3-phase output in fault conditions at output side.AC output with desired amplitude and frequency by connecting directly to DC or AC load.



Figure 10. Three-phase output in fault conditions

4.2. Comparative Analysis

Definitions	DFET	Conventional
Transformer designed	Semiconductor devices	Metal
Bidirectional power flow capability	Yes	Not possible
No.of storage capacitors	1	0
Design simplicity and expandability to achieve higher ratings	Yes,modular structure to any stage	Not possible
Providing neutral wire at the input or output sides at any time required	Yes	Not possible
cost efficient, regarding the design simplicity, the number of DC links capacitors	Good	HVDC devices are required
Reliability regarding independent operation capability of phases	Port, individually	Phases are de- pendent each other
Providing desired voltage and current and connecting in se- ries or connecting in parallel to the grid, suitable for DVR and AF applications	Yes, Same devices	No, Additional devices required
Independent capability of providing desired waveform in each phase , and independent capability of active/reactive power adjustment in each phase for UPQC applications	Yes, Same devices	No, Additional devices required
Transfer of active/reactive power from one phase to another phase or from one line to another line in power distribution system act as IPFC	Yes, Same devices	No, Additional devices required
Providing symmetrical loads voltage from an asymmetrical DC/AC sources for UPS application	Yes, Same devices	Not possible
Management of variable low-voltage DC sources suitable for renewable energy applications	Yes, Same devices	Not possible
fault in Phase	Device work on other Phase	Device stop working
fault clearing	online	Not possible

Table 1. The Performance Study of DFET and Conventional Transformer Method

A comparison study is given to clarify the advantageous and disadvantageous of the DPET. A hree-phase system, contains six ports, is compared to the similar PETs. First, some of the pros and cons of bidirectional DPET in comparison to the unidirectional topologies should discuss. In the unidirectional systems, input power factor is not controllable but in bidirectional structures input or even output power factor can be adjusted. This means that the reactive and active power of each port can be regulated. Also for DG systems like wind turbine, bidirectional capability is indispensable. Energy management for energy efficient systems is another application of this feature. A detail comparison study (e.g., cost, efficiency, quality, etc.) is given in Table 1 to clarify the pros and cons of DPET. In addition, Table 5 shows some of the most noticeable applications of DPET. Dynamic voltage restorer (DVR) and active filter (AF) applications can be satisfied by the FPET, because it can connect to the grid in series or/and in parallel. Desired voltage and current can provide by the flexibility of FPET in providing various waveforms.

5. CONCLUSION

Based on the requirement of a power conversion system, PET is proposed to facilitate many requirements that are expected in power electronic and distribution systems. The proposed topology is flexible enough to provide bidirectional power flow and has as many ports as it is required. For low-voltage application, PET can correct power factor and can adjust the waveform and frequency of the output voltage. The proposed topology can be expanded for high voltage and high current applications. The dc link plays a significant role to provide energy balance, power management in the circuit and independent operation of ports. The PET is extremely modular and can be extended for different voltage levels and power levels. It performs typical functions and has advantages such as power factor correction and double galvanic isolation between each port, as well as using only one storage element.

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APPENDIX

Appendix 1:DPET parameters & component values used for simulation

Parameter	Value
No.ofinputports	5 Port, series connected
No.ofoutputports	3Port, series connected
f _{tf}	2kHz,transformerfrequency
Lf1,2,3,4,5	4 mH(total20mH)
Cd	2200µF
Cf6,7,8	3 x20µF
L _{f6,7,8}	3 x1.5mH
LoadPF	0.8loadpowerfactor
Load	3 x10kW,3phases
V _{d,ref}	600V
v ₁	1900V _{rms} ,50Hz;Utility
N1,2,3,4,5	1.6,turnsratio
N6,7,8	0.8,turnsratio

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