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A Survey of Multilevel Voltage Source Inverter Topologies, Controls and Applications

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ABSTRACT

Multilevel converters tremendous positive contribution in the field of power electronics and renewable energy has been the reason behind the surge in it research interest. The converter has put hope in the minds of power electronic engineers that a time will come when it will break a record by providing an efficient means of utilising the abundant renewable energy resources. In an effort to report the recent advances in renewable energy conversion technology, this paper presents a review of multilevel voltage source converters that are widely being used in engineering applications. It reports the technological advancements in converter topologies of Flying Capacitor (FC), Neutral Point (NPC) /Diode Clamped, and Cascaded H-Bridge (CHB) with their respective advantages and disadvantages. Recent customized/hybrid topologies of the three-phase multilevel inverter with reduced component count and switching combination are reported. The paper also reviewed different modulation techniques such as the multilevel converter carrier base PWM, Space Vector Modulation techniques (SVM), and Selective Harmonic Elimination method (SHE-PWM). Finally, various multilevel converters areas of application were highlighted. This review will expose the reader to the latest developments made in the multi-level converters topology, modulation techniques, and applications.

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1. INTRODUCTION

Over dependency on fossil fuels as the major source of energy poses a serious threat to the continued existence of life on our beloved planet "Earth". The number of greenhouse gases emitted into the atmosphere on daily bases as the result of energy generation and industrial utilisation is quite alarming. Fossils exploration and processing results in severe environmental pollution (both land and water), which entails affects the natural structures and habitat living in them. As the result of the problem above, researchers have focused their attention and resources towards finding an alternative and sustainable means of energy generation that has zero or minimum environmental de-gradational effects compared to the conventional fossil fuels [1]. To this effect, many power electronic converters were designed and had already been placed at various distributed generation (DG) and grid-connected networks [2].

Multi-level converters have become an exciting research area for many power electronic engineers and scientist; this could be mainly due to its high power handling capability making it suitable for both medium and high power industrial applications. Figure 1 below depicts a graphical representation of the significant areas of application. A number of research articles were published on the industrial applications of multi-level converters especially the ones found in high power ac drives systems like electric trains, power

generation stations, crane conveyors and refineries [3]. In addition to its high power handling capability, it also produces a better output voltage waveform closer to sinusoidal, with low output harmonic distortion and reduced switching stress dv/dt on the power electronic switching devices [4]. These features have remarkably put it on top of its conventional counterpart.

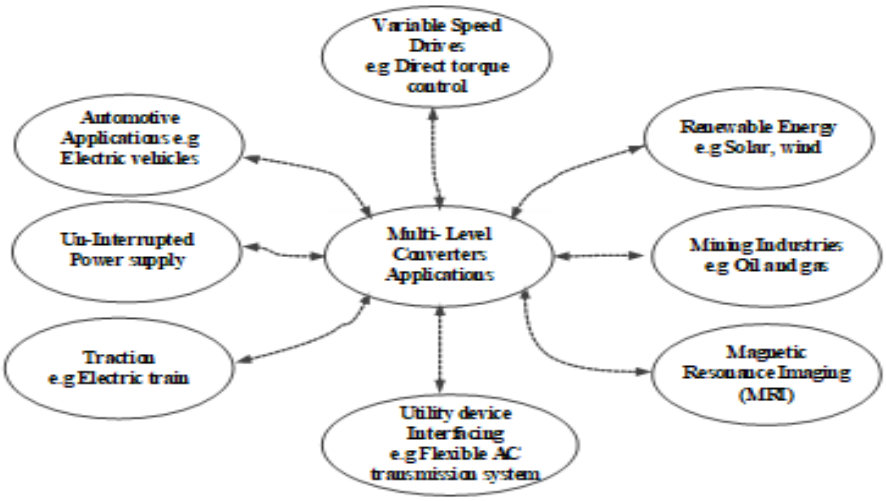

Figure 1. Multi-level inverter converter applications

Multi-level converters can be categorised into three main topologies namely Flying Capacitors (FC), Neutral Point (NPC) /Diode Clamped and Cascaded H-bridge (CHB) [5]. They are invented to increase the inverter output power and at the same time provide solutions to the inability of the ordinary conventional inverters to withstand high switching frequency, high voltage and current stress which cumulatively lead to reduced efficiency and induces substantial electromagnetic- interference (EMI) in the system [6].

The topology composed of some number of low voltage devices, arranged in such a way to share the voltage/current stress across them, which is achieved by employing proper switching sequence on the switches. An essential advantage of multi-level configuration is that without increasing the switching frequency or output power, the harmonics in the converter output are reduced. The word multilevel converter starts from three-level upward and as the level increases the total harmonic distortion (THD) decreases. Voltage problems, clamping requirements, cost and other constraints limit the number of achievable output voltage steps. Switching strategy plays a significant role in the performance of an inverter because it has a direct link to the harmonic content of the inverter output voltage. That is why power electronic scientist has suggested innovative techniques to minimise harmonic distortions in the converter output. Numerous modulation methods such as Sinusoidal Pulse Width Modulation Techniques (SPWM), Space Vector Modulation Technique (SVM) and Optimized Harmonic Stepped Waveform Technique (OHSW) are embraced [7].

The SPWM and SVM techniques were designed to operate at a high switching frequency, which has the merit of reduced output filter size and de-merit of increased device switching stress and heat loss. OHSW technique operates the power devices at a low frequency, exerting less switching stress on the switches; therefore dissipate less amount of heat. The reduced switching frequency results in increased output harmonic distortion, which warrants the need for a large filter size. To realise a smaller size filter using this technique, the dominant low-frequency harmonics needs to be shifted further to a high frequency using step modulation and multiple level inverters, these results in increased inverter price and circuit complexity. To address this problem, a different approach was introduced, were by notches are superimposed on the output waveform at a predetermined angle; this pushed the low order dominant harmonics to a higher frequency so that they can be easily eliminated using a small sized filter [8]. This new approach is called Selective Harmonic Elimination Method or pre-calculated modulation technique. Patel et al. [9] were the first to propose it. This is a non-carrier based technique because it only requires some pre-calculated angles that are stored in a lookup table (memory) [10]. These angles are found by solving the transcendental non-linear equation found through Fourier series expansion of the output voltage equation.

2. MULTILEVEL VOLTAGE SOURCE CONVERTER

As previously stated, quite a number of multi-level converter topologies have been mentioned in several kinds of literature [11]. In this paper, the three most promising topologies that serve as the base for hybrid configurations are reviewed in detail. The high voltage capability, fewer harmonics in the output waveform and higher efficiency are some of the advantages that made multilevel voltage source noteworthy [12]. A common drawback to the multilevel inverters is its complexity and cost due to the need for more number of power switches [13]. Figure 2 summarizes the various classifications of high power converters.

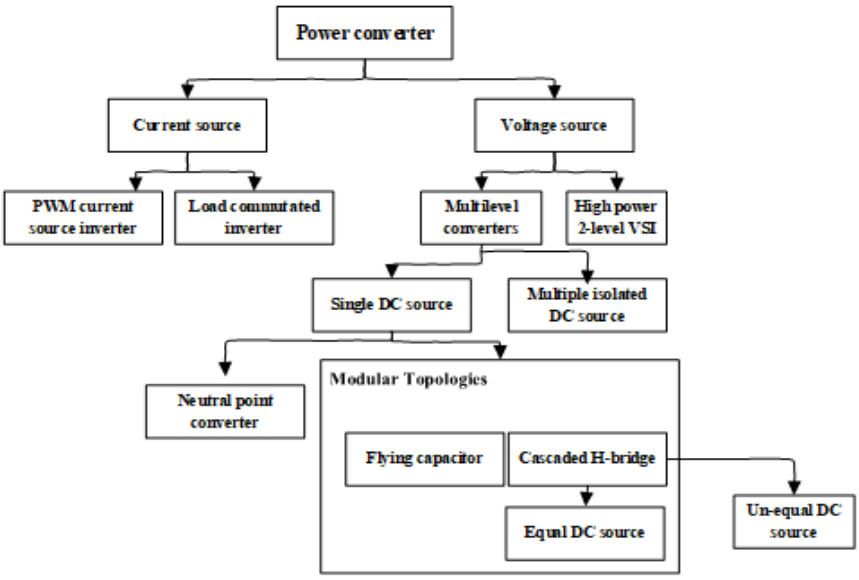

Figure 2. Converter classifications

2.1. Converter terminologies

Here, some commonly used terminologies and assessment parameters in the field of multi-level power converters are highlighted.

a. The reduced device counts multi-level inverter (RDC-MLI): Refers to the topology in which for a given number of phase level the number of controlled switching devices are reduced.
b. Total voltage blocking capability: Refers to the maximum amount of reverse voltage the converter switches are capable of blocking [14].
c. Symmetric and asymmetric source configuration: The term symmetric in an MLI refers to when the voltages of the input dc level are equal; otherwise, it is termed asymmetric [15],[16].
d. Even power distribution: Also known as charge balance control or equal load sharing [17]. When each input source of a multilevel conversion provides equal power to the load, such power distribution within the sources is said to be 'even'. In some literature, it is called charge balance control or equal load sharing.
e. Level- Generation and Polarity-Generation: MLI generates stepped output waveform by controlling the dc input source in such a way that it adds up and subtracts to produce a level waveform. The generated output composed of both positive and negative polarities, allowing the realisation of an alternating signal with positive and negative half cycle. The MLI converter switches in the polarity generation circuit have to be able to withstand the operating voltage.
f. Fundamental frequency Switching: It is a frequently mentioned converter terminology. It is known that switching frequency, current and blocking voltage are proportional to the switching losses in a converter [18]. To minimise the losses, the MLI is operated at low frequency, which is called fundamental frequency while reserving the output quality.

2.1.1. Converter assessment parameters

The performance measurement of any multilevel inverter topology is based on how well it performs on the application in which it is meant for. The performance assessment of reduced device count multi-level converters with regards to other topologies can be based on the following parameters:

a) Blocking voltage of the converter

b) Controllability of the topology
c) Total number of the power switch
d) Ability to employ asymmetric voltage ratios

2.2. Conventional Topologies

This section discusses the three conventional topologies within which most of the current hybrids are drawn from.

2.2.1. Diode Clamped Topology

Diode clamp multi-level converter topology is an advancement of a three-level Neutral point inverter invented in the early 80's [19]. Later in the 1990s, the number of steps was increased up to six levels [20]. Clamping diodes are used in this type of converter to reduce the device voltage stress. An m_d level diode clamped converter needs $(2m_d - 2)$ switching device, needs $(m_d - 1)$ input voltage source and $(m_d - 1)$ $(m_d - 2)$ number of diodes with a voltage Vdc across the diodes and switch [21]. Figure 3 shows single-phase 5-level diode clamp converter. It comprises of four series connected capacitors in parallel with the Dc bus. The Dc bus input voltage V_{dc} is shared equally across the four capacitors, each having $\frac{V_{dc}}{4}$ across it. The number of series connected capacitors determines the output voltage step. For M steps diode clamp inverter, there are M-1 series connected DC bus capacitors. The clamping diodes have different voltage ratings depending on its position in the circuit. Diode D3 in the figure should at least be able to block $\frac{3V_{dc}}{4}$ voltages were D1 will only block $\frac{V_{dc}}{4}$ [4]. Table 1 below shows the possible output voltage steps between point Vx and Vo, with their allowable switching combination. Logic state1 and 0 corresponds to the switch On and Off states.

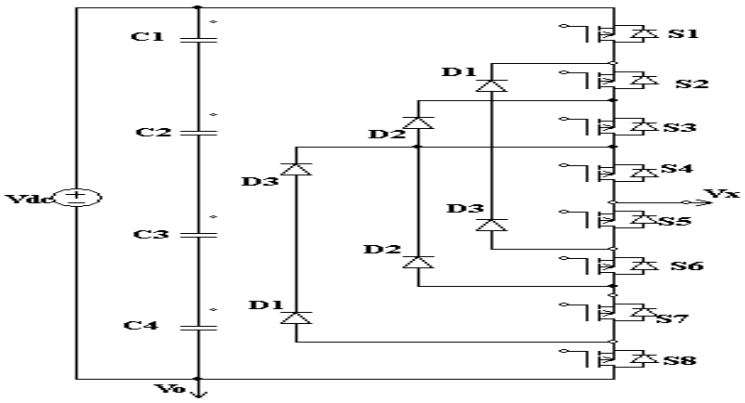

Figure 3. 5-level diode clamp converter

Table 1. Diode-clamped Voltages with their corresponding switching combination

Voltage	Switching States							
$\mathbf{V_{ox}}$	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$\mathbf{V_1}$=0	0	0	0	0	1	1	1	`1
$\mathbf{V_2} = \frac{V_{dc}}{4}$	0	0	0	1	1	1	1	0
$\mathbf{V_3} = \frac{V_{dc}}{2}$	0	0	1	1	1	1	0	0
$\mathbf{V_4} = \frac{3V_{dc}}{4}$	0	1	1	1	1	0	0	0
$\mathbf{V_5} = \mathbf{V_{dc}}$	1	1	1	1	0	0	0	0

From the table, it can be seen that switch (S_1, S5), (S_2, S6), (S_3, S7) and (S_4, S8) are operated complementary and in a sequential switching pattern. Each of the switching devices should at least be able to block $\frac{V_{dc}}{4}$ voltage level. The clamping diodes blocks unequal reverse voltage. For instance, when the converter output voltage is at $V_1 = 0$, all the lower arm switches are said to be at On state, in this case D3 has to block $\frac{3V_{dc}}{4}$, D2 blocks $\frac{V_{dc}}{2}$, and D1 will block $\frac{V_{dc}}{4}$. In a situation where a converter is to be designed with the

same rated diodes, then for a Dn-1 positioned diode, n-1 series connected diodes will be required to block $(n-1)\frac{V_{dc}}{n}$ reverse voltage [4]. Below is the list of advantages and disadvantages of diode clamped converter topology [22].

Advantages:	Disadvantages:
1. It requires single isolated Dc supply; this warrants the possibility of having a back-to-back connection. 2. The Dc bank capacitors can be charged simultaneously. 3. It provides a better efficiency when operated at the fundamental switching frequency.	1. The number of clamping diodes increases with increase in voltage level. This brought about the additional cost and circuit complexity, especially in higher steps converters. 2. Unequal switching stress across the switching device, i.e. inner switches conduct for a short time compared with the inner switches. 3. Not suitable for redundancy.

2.2.2. Flying Capacitor Topology

Flying capacitor (FC) is another converter topology that was invented in the early 90's by Maynard et al. [23]. It circuit connection is similar to that of a diode clamp, only that capacitors were placed instead of diodes. An m level diode clamped converter needs $(2m-2)$ switching device and needs $(m-1)$ number of capacitors with a voltage Vdc across the `capacitors and switch [21]. Figure 4 shows its 3-phase circuit connection. The topology comprises of a ladder-like arranged dc link capacitors, each having a different voltage rating. The voltage difference between two adjacent capacitors determines the amplitude value of each step. To generate M-level phase voltage steps at Vxo, M-1 capacitors need to be connected serially at the dc-bus. The line voltage Vxy, in this case, will be (2M -1) levels. One of the benefits of flying capacitor over diode clamp is its redundancy property. It can generate a particular output voltage using multiple switching sequences. For an M-level flying capacitor converter designed with equal rated capacitors, the number of phase capacitors can be found using the expression ((M-1)(M-2))/2 [19].

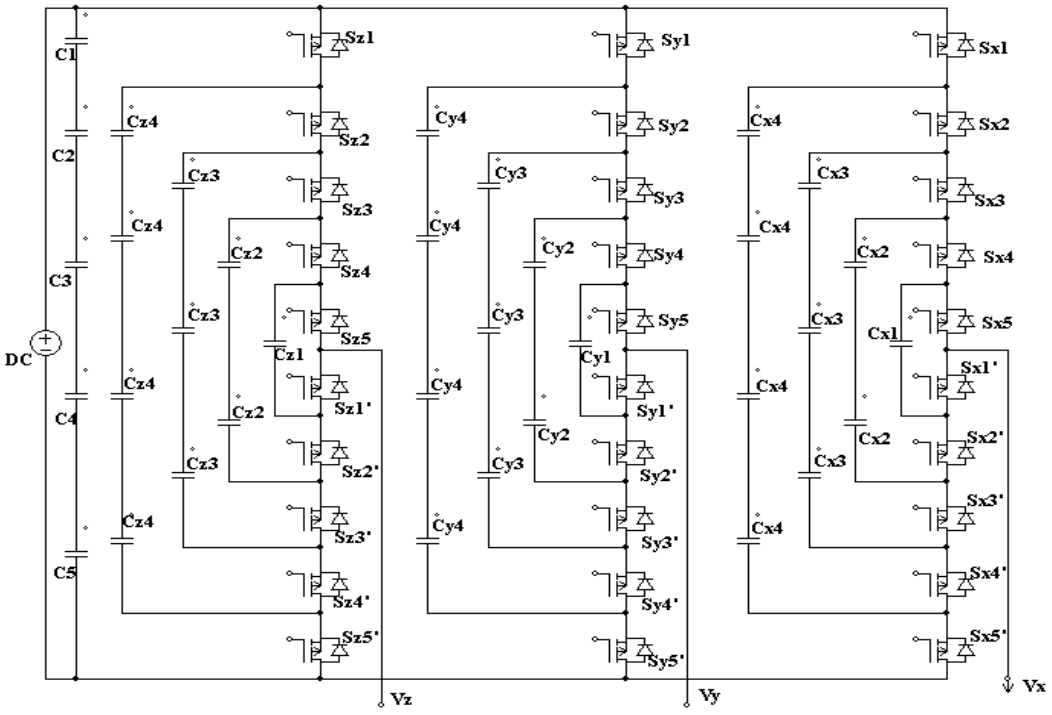

Figure 4. Five-Level Flying capacitor Multilevel converter

The merits and demerits of the multi-level flying capacitor are stated as follows [19].

Advantages:	Disadvantages:
1. High-value capacitors can serve as a backup during a power failure and voltage sagging. 2. The topology allows the possibility of switching redundancy, which results in voltage stress balancing across the capacitors. 3. Allows the control flow of real and reactive power. 4. It requires single isolated dc supply voltage source.	1. The number of capacitors is determined by the inverter output level. This makes the circuit looks bulky and difficult to package. 2. A complex control mechanism that requires feedback is involved. This is to maintain voltage across the capacitors. 3. The converter has poor efficiency due to high switching losses.

2.2.3. Cascaded H-bridge Topology

A cascaded H-bridge is a promising converter topology made up of series a connected H-bridge inverter module. Figure 5 shows a single phase 5-level circuit configuration of the inverter. The circuit comprises of four full bridge modules with each having its independent dc supply. The nine-level voltage steps are generated by adding up the individual output voltages generated by each module. By employing a systematic switching function on the switches, each of the H-bridge cells can synthesise three different voltage levels, positive (+E), zero (0) and negative (-E) [3]. The sequence of phase voltage steps is expressed in a unique and distinctive pattern from the earlier mentioned topologies. In this case, it is express as $N= 2P_{dc}+1$, where P_{dc} stands for the number of independent Dc source.

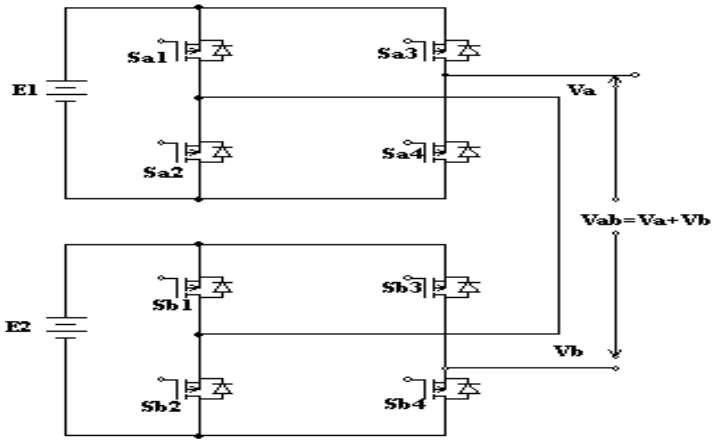

Figure 5. Single phase 5-level Cascaded H-bridge Converter

From the Figure 5, switch S_{a1} and S_{a2} are called the converter leg and are always operated complimentary to avoid short-circuiting the supply. The five-level switching sequences and their corresponding output voltage is given in Table 2.

Table 2. The five-level Cascaded H-bridge Converter switching sequences

Voltage	Switching States							
V_{ab}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
V_1=-2E	0	1	1	0	0	1	1	`0
V_2 =−E	0	1	1	0	0	1	0	1
V_3 =0	0	0	0	0	0	0	0	0
V_4 =+E	1	0	0	1	1	0	1	0
V_5 =+2E	1	0	0	1	0	0	0	1

Out of the three mentioned topologies in this paper, cascaded H-bridge topology uses the least number of power electronic components. The advantages and disadvantages of this topology are summarized as follows [3].

Advantages:	Disadvantages:
1. There is an automatic voltage sharing across the switches in a module due to the usage of the independent voltage source. Therefore, reduces restriction in the switching sequence. 2. The converter produces more output voltage levels, providing a smooth and steady voltage change across the load, resulting in less THD for a particular operating frequency. 3. Its modular nature makes its production, maintenance and redundancy integration much easier. 4. Higher voltage level can be achieved by series-connecting more H-bridges.	1. The need for separate independent dc supply by each of the H-bridge modules. Increases the device cost and size.

3. HYBRID CONVERTER TOPOLOGIES WITH REDUCED DEVICE COUNT

This section reports three phase-modified topologies with reduced device count. Some of this topologies are hybrids or a slightly modified existing configuration.

3.1 Three-phase Multi-level DC link inverter (MLDCL)

This is an inverter circuit proposed by Rao et al. [24], it associated gate drive circuitry was reduced as it utilizes fewer switches in contrast to the 36 switches in the conventional three-phase cascaded inverter topology. For m number of voltage level, MLDCL requires m+3 active switches per phase, which is half the number of switches and clamping diode required in diode-clamped topology and also half the voltage capacitor and clamping capacitors needed in flying capacitor topology. Figure 6 below shows the circuitry of the proposed hybrid MLDCL converter.

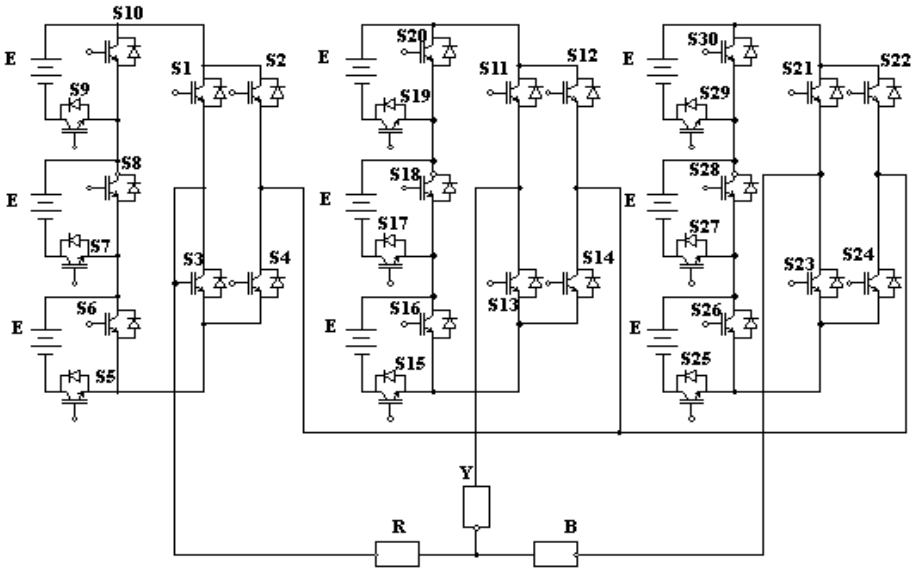

Figure 6. Three phase Multilevel DC link inverter topology

Sub-harmonic and modified space vector pulse width modulation are the control techniques used in the proposed topology. Table 3 shows the proposed topology single phase switching states and the respective generated voltage.

Table 3. Switching States for a single phase seven level MLDCL inverter

V_0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
0	1	0	0	1	0	1	0	1	0	1
E	1	0	0	1	0	1	0	1	1	0
2E	1	0	0	1	0	1	1	0	1	0
3E	1	0	0	1	1	0	1	0	1	0
-E	0	1	1	0	0	1	0	1	1	0
-2E	0	1	1	0	0	1	1	0	1	0
-3E	0	1	1	0	1	0	1	0	1	0

3.2 Three-phase Reduced Switch Multi-level Inverter (RSMLI) Topology

This topology produces a seven-level output voltage that is almost sinusoidal, thereby reducing the converter lower order harmonics. The converter uses three H-bridge modules with one module per phase and 3 additional connected switches that allows the possibility of achieving the desired seven level waveform. There are a total of 21 switches and 9 dc sources with three each per phase. In order to determine the switching angles for generating a fundamental output voltage, it uses fundamental switching scheme. Below is the circuit of a 3-phase 21 switch MLI [25].

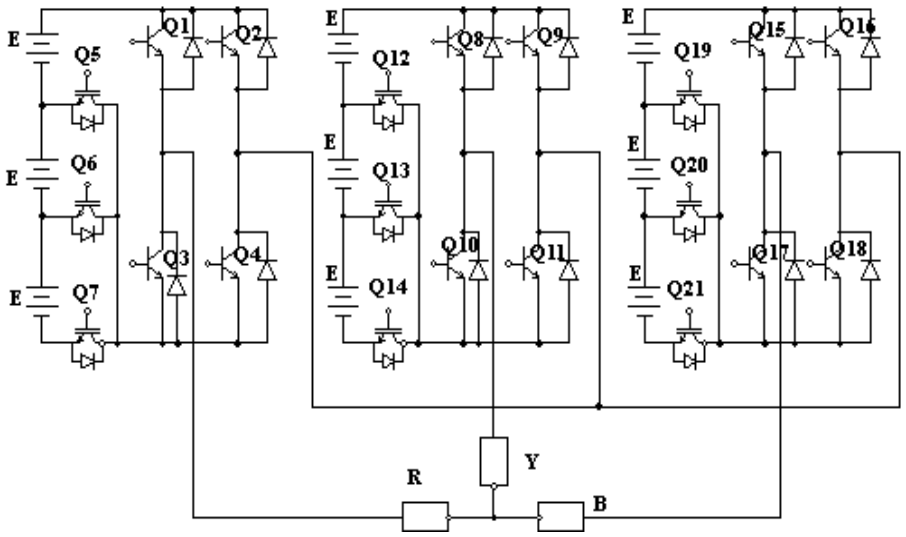

Figure 7. Three phase seven level Multilevel Inverter

The proposed topology has three operating modes, namely; powering mode, freewheeling mode and regenerating mode. For the powering mode, the load current and voltage polarities are the same. In the freewheeling operating mode, one of the main switches is off and passage of the load current is due to load inductance, whereas in regenerating mode the stored energy in the load inductance is feedback to the source, the load current has to be positive during the negative half cycle and negative for positive half cycle [25]. Table 4 shows the per phase switching states of the power electronic switches and the corresponding generated output voltage. The same switching combination applie to the remaining two phase.

Table 4. Switching states per phase for seven level Inverter

Switches in ON states	Output voltage [$V_{ao}(t)$]
Q_1, Q_4, Q_5	E
Q_1, Q_4, Q_6	2E
Q_1, Q_4, Q_7	3E
$Q_1, Q_2,$	0
Q_2, Q_3, Q_5	-E
Q_2, Q_3, Q_6	-2E
Q_2, Q_3, Q_7	-3E
Q_3, Q_4	0

3.3. Reverse Voltage Multilevel Inverter Topology (RVMLIT)

Najafi and Yatin [26] proposed a new MLIT that has dual operational functionalities. The first part utilizes high-frequency switches for the generation of level states, and the second part employs low frequency for the generation of the polarity of the output voltage. Therefore, these two high and low frequencies produce the required output voltage. To generate a seven-level output voltage, two different topologies are integrated per phase, which requires 10 switches in a phase. The upper six switches generate the required non-polarized output waveform levels while the lower 4 switches in the full bridge circuits do generates the polarity. Duplicating the middle stage increases the output voltage level. As seen from the circuitry, to generate a particularly desired polarity, the output voltage is the input to the full bridge converter with the converter output fed into the primary of a transformer whose secondary is arranged in the delta and to the three-phase system. The circuit diagram is shown in Figure 8.

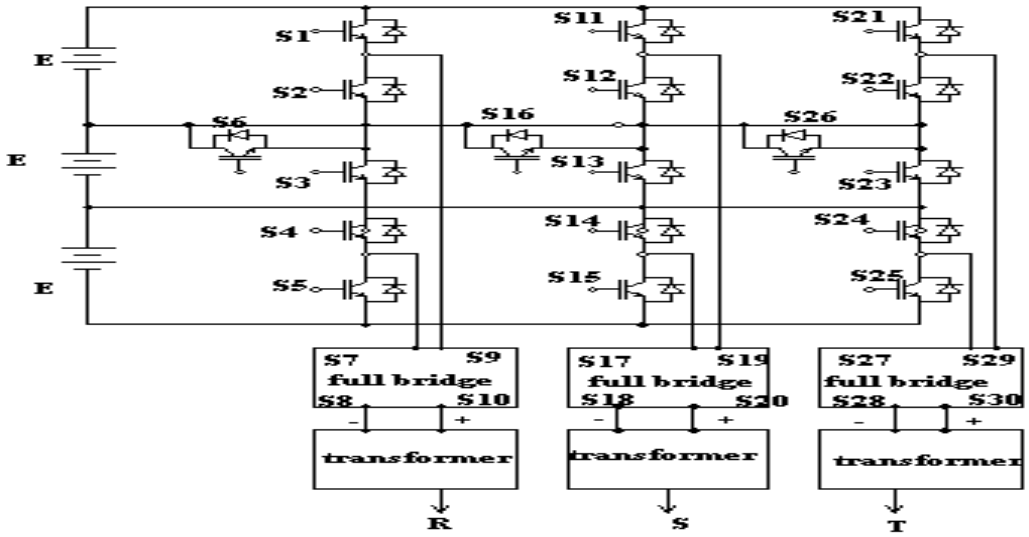

Figure 8. Reverse voltage multilevel inverter topology

3.4 Three-phase Asymmetrical Cascaded Multilevel Inverter Topology (ACMLIT)

The converter is called asymmetrical cascaded MLIT due to its unequal magnitude of the input DC sources. This MLI topology can be integrated with renewable energy sources as it requires less number of DC sources [27]. Figure 9 shows the circuit diagram of the asymmetrical cascaded topology.

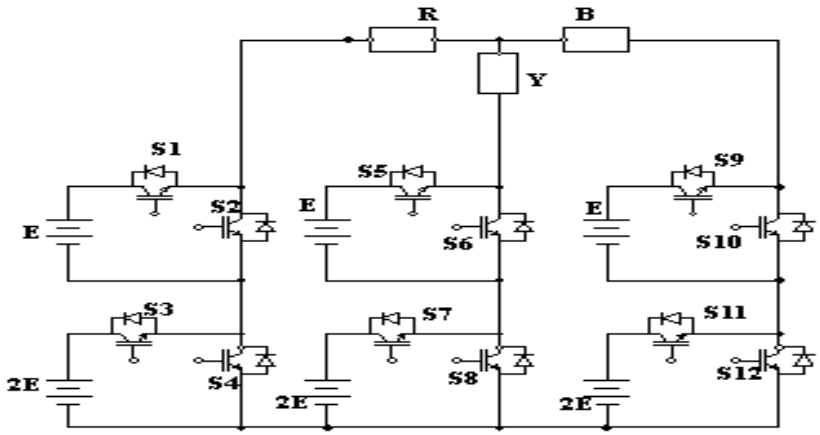

Figure 9. Three phase Asymmetrical Cascaded Multilevel Inverter Topology

The zero and E-level output voltage level are generated using two switches and a single DC source. In order not to short-circuit the DC source, the switches S_1 and S_2 are operated in a complementary manner. The two DC sources and four switches of each phase of the proposed topology forms a module structure. Three basic unit can be added based on the required output voltage levels. It generates the PWM signals through comparison of the reference sine wave with the carrier wave thereby generating pulse signals A_1, A_2, A_3.

3.5. Three-phase Symmetrical Multilevel Inverter Topology (SMLIT)

This is another modular 3-phase symmetrical topology, which produces 3-phase output voltage level using 12 switches [28]. Each phase comprises a battery and two switches in series and parallels respectively. Both switches connected to the battery are operated in complementary to each other. Increasing the number of phase elements (components) increases the number of the voltage step.

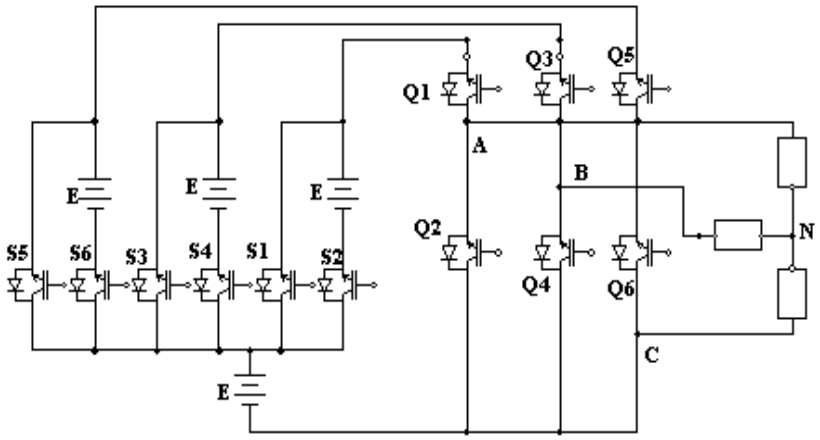

Figure 10. Three-phase Symmetrical Multilevel Inverter Topology

Equation 1 to 3 shows an expression of this topology that outlines the relationship between the number of cells, output levels, power electronic switches.

$$M_{level} = 2Ncell + 3 \quad (1)$$

$$N_{sw} = 3(2Ncell + 2) \quad (2)$$

$$N_{ps} = 3Ncell + 1 \quad (3)$$

Where M_{level} = number of output levels, N_{ew} =number of power switches, N_{ps}=number of power electronic switches, N_{cell}=number of cells

3.6. 5-level three-phase cascaded hybrid Multilevel inverter

Thongprasri [29] proposed a three-phase cascaded hybrid multilevel inverter comprising of a 3-phase inverter in series with an H-bridge module. Each module has a separate independent dc source. He uses multi-carrier based modulation sub-harmonic PWM (MC-SH PWM) on FPGA board to generate the control signals. Figure 11a shows the 3-phase topology of the proposed multilevel inverter.

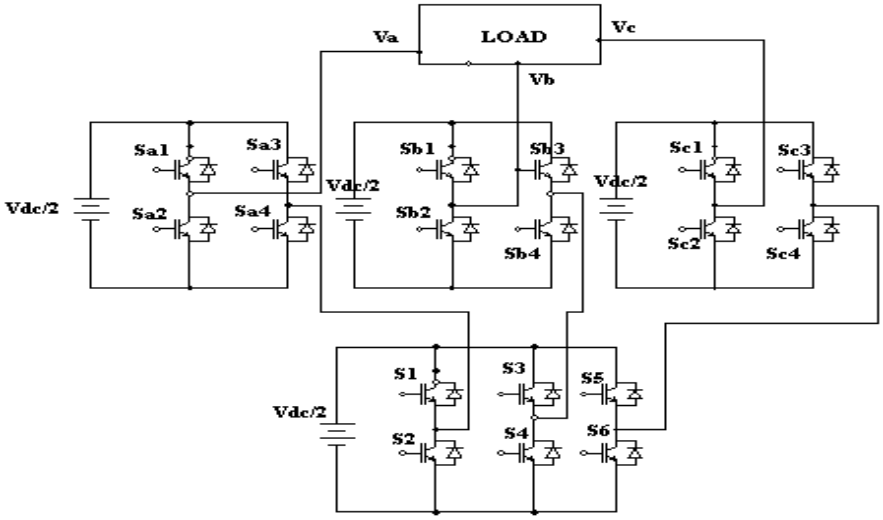

Figure 11a. 5-level three-phase cascaded hybrid multilevel inverter

The proposed topology was tested using 3 different types of the load; 18W fluorescent lamp- ballast, RL, and 1HP 3-phase induction motor; without filtering. The per-phase circuit configuration is given in Figure 11b.

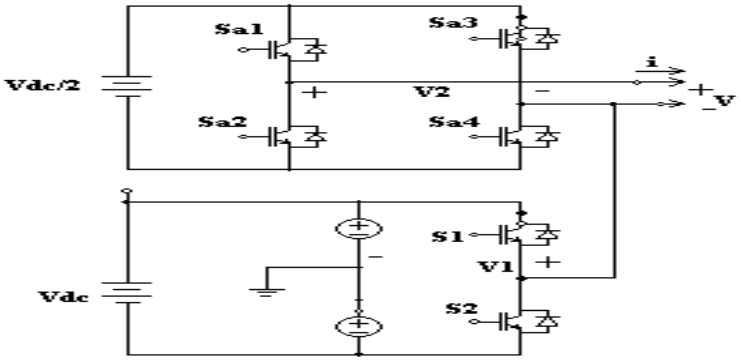

Figure 11b. 5-level Single-phase cascaded hybrid multilevel inverter

4. MULTILEVEL CONVERTERS MODULATION TECHNIQUES (MT)

Due to the rapid advancements in the field of power electronics and the tremendous breakthrough and confidence poised by multi-level converter technology, researchers are exploring every aspect of it, with the aim of improving its overall performance. With the subsequent invention and modification of topologies, the need for new and compatible modulation techniques to suit the new topologies can never be overemphasized. This is the reason why modulation technique is trending in the field of power electronics

[3]. The ever-rising complication of power control systems as the result of additional auxiliaries, the need to reduce switching losses and stress on individual power switches, have facilitated significantly in the advancement so far recorded
in the field of modulation techniques [30]. Several techniques have been developed with each having its merits, de-merits and preferential area of application. Figure 12 shows the various classifications of multi-level converter modulation techniques. From the figure, it can be seen that the techniques are categorized into two broader groups based on their domain of operation. These are the state space vector techniques and the voltage level based approach [31]. The former operates based on the voltage space vectors while the latter operates on voltage level over a period of time.

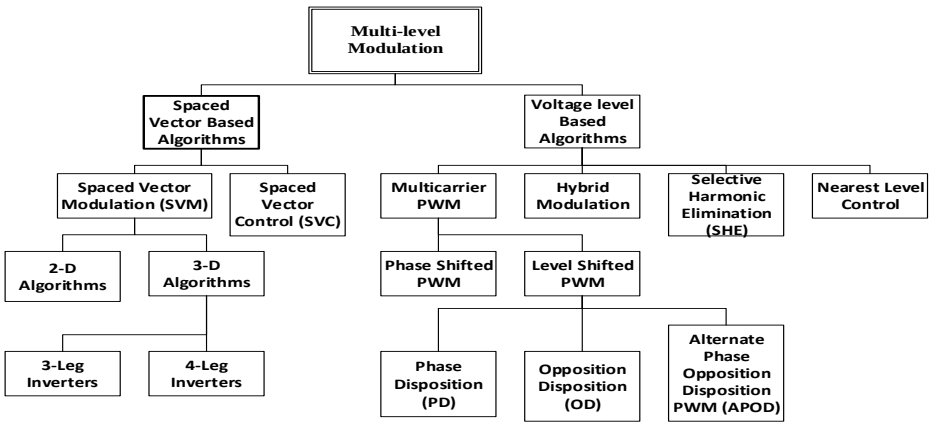

Figure 12. List of Multilevel converter Modulation techniques

4.1. Carrier Based Pulse Width Modulation (CB-PWM)

The early PWM techniques were transformed and upgraded to be applied to the current multi-level topologies. The new technique unlike the conventional counterparts produces the control signal using multiple carrier signals, hence called multi-level PWM [32]. FC and CHB topologies can both be configured in modular form, hence giving the leverage for each module to be modulated independently using bipolar and unipolar sinusoidal carrier PWM, this amount to equal power distribution in the module cells. An N cell of FC and CHB will require (180°)/N and (360°)/N carrier phase shift respectively to generates a low harmonic distorted multi-level voltage waveform [33]. This technique is denoted as Multi-level Phase Shift Sinusoidal Pulse Width Modulation (MPSSPWM). Its major advantage is its ability to suppress the harmonics at the inputs of CHB's converters and also it can provide a balanced dc voltage in FC converter topologies. A new different approach called Level Shift Pulse width modulation (LSPWM) was introduced, it requires superimposing two carrier signals on each other. This technique is further sub-classified into 3 categories namely Alternate phase opposition (APOD), Phase opposition disposition (POD-PWM) and Phase disposition (PD) on the bases of the spatial orientation of the carrier signal [32].

4.2. Space Vector Modulation (SVM)

This technique involves comparison of converter gating signal with the vector representation of a sinusoidal reference (V_{ref}), whereby a replica of the reference voltage is reproduced at the converter output [33]. SVM technique is currently applied on various converter topologies, resulting in the development of new algorithms that suits the existing topologies, this can be seen in the various reported literature. The reported techniques are application specifics that are designed to work on a fixed converter output steps. The higher the output steps, the more complex the control algorithms and the mathematical computations. The drawback poised by the complex algorithms and rigorous computations was later addressed in the subsequent literature [34].

Franquelo et al. [35] in his article "Space vector modulation technique for multi-level converters", proposed a new algorithm that uses simple computational procedures to produce a reference value close to the state vector, hence eliminating the need for lookup tables. In addition to reducing tedious computations, it also disputes the notion that says the more the output steps, the more the computational complexity. In another literature, a new 2 dimensional modified SVM (MSVM) technique was presented in [31]. The technique is suitable for application in 3-phase balanced system where all triple harmonics have cancelled. A

more sophisticated algorithm that warrants an online vector calculation was presented in [36], it is called 3 Dimensional algorithms because it is an upgraded version of the earlier discussed 2D, it has further minimised mathematical computations and eliminates the links between circuit complexity and converter output step. This technique applies to both balanced and unbalanced systems [36].

4.3. Selective Harmonic Elimination Method (SHE-PWM)

Another name given to this modulation technique is offline or pre-calculated modulation technique. It was first proposed by Patel et al. [9]. This is a non-carrier based technique because it only requires some pre-calculated angles that are stored in a lookup table (memory) [37]. These angles are generated by first finding the Fourier expansion of the voltage waveform, which happens to be a non-linear trace-dental equation as shown in equation (4).

$$H_n = \begin{cases} \frac{4*E}{n\pi}\left\{(-1)^N\left(1+2\sum_{K=1}^{N}(-1)^K cos(n\alpha_K)\right)\right\} & for\ odd\ n \\ 0 & for\ even\ n \end{cases} \quad (4)$$

Based on the odd quarter wave symmetry theory, the dc components and even harmonics will cancel out will be left with the fundamental and odd harmonic components [38]. The fundamental component is equated to a constant value which is determined by the selected modulation index, and the odd harmonics are equated to zero. The generated equations have no direct solution. Hence, numerical techniques which involve iterative procedures as in Newton Raphson method [39]. Mathematical resultant method, which uses the concept of polynomials, optimization techniques or Hybrid genetic algorithm, are capable of providing an approximate value of the angles [10]. SHE method has drastically reduced switching loss, which is the reason why it has been extended to high power multi-level converters [37].

Its drawback is its restrictions to open loop systems and the complexity in finding the switching angles for a higher number of steps. These limitations resulted in the invention of other low switching loss techniques with feedbacks that are suitable for higher level applications [31].

4.4. Sinusoidal PWM (SPWM)

This technique works based on the comparison of a referenced sinusoidal wave and a triangular carrier wave. The output voltage waveform is formed as a result of the gating signal been fed into the inverter switches. These gating pulses are formed when the reference wave is larger than the carrier wave as depicted in the figure below [40].

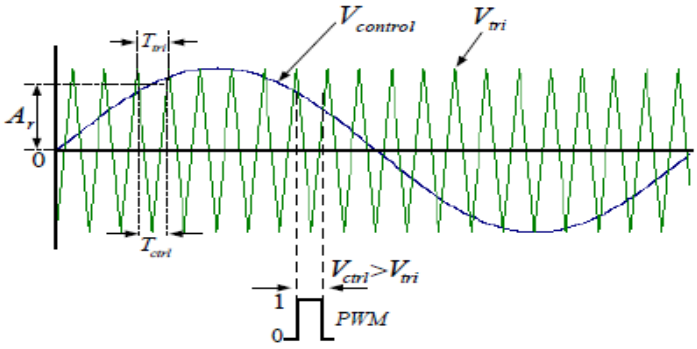

Figure 13. Pulse generation using reference and carrier signal

4.5. Phase Disposition (PD) PWM

This technique enhances output voltage of a multi-level converter by optimally suppressing the output harmonics. Hence, minimising the distortion level in the voltage waveform. It employs several optimisation techniques, the likes of gradient optimisation algorithms [41].

4.6. Staircase Modulation

The staircase modulation method is most suitable for elimination of device stresses and switching losses in higher voltage and power energy conversion. It does so by determining the optimal primary values

of the switching angles. Particle Swarm optimising algorithm can be utilised in solving the transcendental equations because it makes the switching angle solution converges at the global minimal [42].

4.7. Stepped Modulation

Here, the modulating signal is a stepped waveform, divided into intervals with each interval controlled separately to minimized specific harmonics. Converters controlled using this technique has less distortion compared to the conventional PWM modulation method [40].

4.8 Comparison of Modified/Hybrid Three Phase Multilevel Inverter Topologies

With the aim of keeping the THD within the standard limit and lesser device count, researchers have proposed different control strategies. Table 5 shows the comparison of some of the hybrid/ modified three-phase topologies based on modulation techniques, number of diodes and switches, Dc source and percentage of THD in the output.

Table 5. Three phase converter topology parameter comparison

S/N	Author	Topology	N_s	N_d	N_c	N_{dc}	N_t	MT	THD
1	[43]	BDSI	6	0	2	1	0	PWM	25
2	[44]	CCHB	36	0	0	9	0	Sub-H PWM	10.78
								MSVM	8.79
3	[30]	HMLIT	18	0	2	4	0	MCSVM	15.6
4	[26]	RVMLIT	30	0	0	3	3	PD PWM	3.85
5	[24]	MLDCLT	30	0	0	9	0	Sub-H PWM	9.02
								MCSVM	6.84
6	[26]	RSMLIT	21	0	0	9	0	SHE PWM	7.8
7	[28]	ACMLIT	12	0	0	6	0	SPWM	25.609
8	[29]	SMLVI	12	0	0	4	0	LFM	16.88
								SingleCSPWM	34.83
								Two CSPWM	35.35

Note: Some of the notations used in the table are mentioned in the text, the rest stands for the following: N_s stands for the number of switches, N_d number of diodes, N_c number of balanced capacitors, N_{dc} stands for the number of DC inputs, N_t number of transformers, BDSI stands for Bi=derictional switched inverter, CCHB stands for conventional cascaded H-bridge, HMLIT stands for Hybrid Multilevel inverter topology, Sub-H PWM stands for Sub-harmonic Pulse width modulation, LFM stands for Low-frequency modulation, CSPWM stands for Carrier Sinusoidal PWM.

5. CONCLUSION

This paper presented a comprehensive survey on multilevel converters. With emphasis given to the conventional topologies, that serves as the basis of the modern hybrid topologies. Converters operational characteristic, advantages, disadvantages and major areas of applications were outlined. The paper also reviewed some recently proposed three-phase hybrid multilevel inverter topologies with reduced device count and modified switching function. The hybrid topologies appeared to have low total harmonic distortion, less number of power electronic components and an additional number of output steps compared

to the conventional topologies. The paper reported the promising and widely used modulation techniques the likes of multilevel carrier base PWM, space vector modulation techniques (SVM), selective harmonic elimination method (SHE-PWM) and phase disposition (PD) modulation techniques. It is hoped that this review will serve as a source of literature to the vast amount of new researchers in the field of multilevel voltage source converters.

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