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FPGA Based Implementation of Symmetrical Reduced Switch Multilevel Inverter

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ABSTRACT

Multilevel inverter has become more popular and attractive for drive applications. Among the various modulation techniques, Carrier based techniques has been commonly used because of their simplicity and flexibility. This paper presents the comparisons of bipolar multicarrier pulse width modulation for the new symmetrical multilevel inverter. The performance parameters of new multilevel inverter were analyzed through various switching strategies. The detailed study has been carried out by MATLAB/SIMULINK. The real time implementation was carried out using FPGA. The results of both simulation and experimentation were compared.

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1. INTRODUCTION

A multilevel inverter is a power electronic system that synthesizes a desired output voltage from several levels of DC voltage as inputs. Multilevel Inverter (MLI) is not only achieves high power ratings but also enables the use of renewable energy sources, due to this, industries are mostly preferred this converters. The conventional inverters provide only two level voltage but we get several level from MLI which results in high power quality, lesser harmonic components, improved electromagnetic compatibility and lower switching losses. The main objective of multilevel topologies is the increase of power, the fall in voltage stress on the switches and the generation of excellence output voltages and sinusoidal currents. Different topologies are proposed namely DCMLI, FCMLI and CHBMLI. These topologies are differing by the operating mechanism.

Many modulations techniques have been developed like fundamental switching method, pulse width modulation, selective harmonic elimination and space vector modulation etc. Out of these techniques, PWM techniques have been widely used because of their ease and litheness. Carrara et al discussed control freedom degrees combination and their analysis for PWM methods. Mohan et al discussed the single triangle PWM method and its variants are effective for controlling the inverters. Agelidis and Calais proposed carrier based multilevel PWM method which effectively control the diode clamped inverter. Martina Calais et al analyse the multicarrier schemes by applied in cascaded multilevel inverter. Aziz described the digital simulation study for modular structured multilevel inverter. Krein et al introduced modified carrier approach and it can be minimizing harmonics. Jana et al presented switching pattern for cascaded MLI based on space vector modulation technique. Mekhilef et al discussed the symmetrical digital pulse width modulation technique. Dahidah and Agelidis suggested that the selective harmonic elimination pulse width modulation is suitable

for high power applications. Haiwen et al compared the fundamental switching method with pulse width modulation method by applying in cascaded multilevel inverter. Roozbeh Naderi and Abdolreza Rahmati developed phase shifted carrier PWM technique for cascaded inverters. Krishna described the conventional multilevel inverter to produce small voltage steps and series capacitor also used for voltage balance. Najafi et al proposed the reversing voltage topology for multilevel inverter. Babaei proposed cascaded multilevel inverter topologies with less power semiconductor devices. Ersoy Besery et al developed new symmetrical multilevel inverter with reduced switches. Whenever we are providing equal DC voltage sources as input then this type of inverter is mentioned as symmetrical multilevel inverter whereas unequal sources means asymmetrical multilevel inverter.

In this paper a new type of symmetrical multilevel inverter has been analyzed based on performance parameters through various PWM techniques and the simulation results were validated with the help of prototype model.

2. NEW SYMMETRICAL MULTILEVEL INVERTER

More number of switches required for traditional multilevel inverters, due to this circuit cost, installation area and switching losses becomes high and control circuit also complicated. To overcome this problem a new topology introduced in Figure 1.This topology consists of 3 auxiliary switches, 4 main switches, 3 diodes and three DC sources to form seven level. This new topology achieves reduction in the number of main power switches by 42%**.** The next higher level can be obtained by adding a single switch, a diode and a DC source.

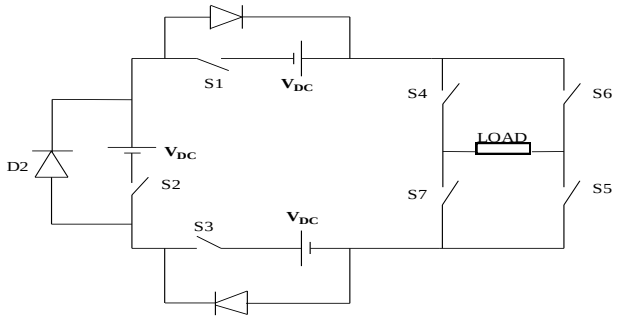

Figure 1. Symmetrical multilevel inverter

In order to obtain $3V_{DC}$ at the output, the switches S1, S2, S3, S4 and S5 were ON. The load is connected between S4 and S5. In this mode, all the three sources were connected in series which produces $3V_{DC}$ at the output. When S2, S3, S4 and S5 were ON and diode D1 conducts, only two sources were in series and generate $2V_{DC}$ .To get V_{DC} at the output, switch S3, S4 and S5 is ON and diode D2 and D1 conducts.

The output voltage levels at the negative half cycle were achieved by connecting the load between S6 and S7 instead of S4 and S5.

3. MODULATION STRATEGY

Bipolar multicarrier based PWM strategies were used to switch the power devices to produce several levels at the output voltage. The PWM based strategies are most popular because of carrier, which controls inverter output voltage thus obtained by adjusting the conducting periods of power semiconductor switches. Carrier based strategies classified as single carrier and multicarrier strategies. Multicarrier PWM strategies such as, Phase disposition PWM, Alternate phase opposition disposition PWM and Carrier overlapping PWM were implement in this paper. Carrier based method operate based on the comparison of modulating signal with carrier signals where carrier signal can be triangular, sawtooth and any other shape based on control freedom degree including amplitude, frequency and offsets between carriers. For getting 'm' levels, m-1 carriers are needed, for bipolar PWM Strategies. The carriers consist of same frequency f_c and same peak to peak amplitude A_c. The modulating signal has amplitude A_m and frequency f_m and is placed at the middle of the carrier set. The frequency ratio m_f is defined. In this paper, the modulating frequency mf is taken as 20, modulating index ma varied from 0.7 to 1.0.

$m_f=f_c / f_m$
The amplitude modulation index m_a is defined as
$m_{a=}A_r /A_c$

3.1. Phase Disposition Strategy

In this strategy six triangular carrier with the identical frequency f_c and peak-to-peak amplitude A_c which are disposed so that the bands they occupy are contiguous. The carrier set is placed above and below the zero reference. The carrier arrangement for seven level inverter using PDPWM is shown in Figure 2. for m_a=0.8 and $m_{f=}$20.

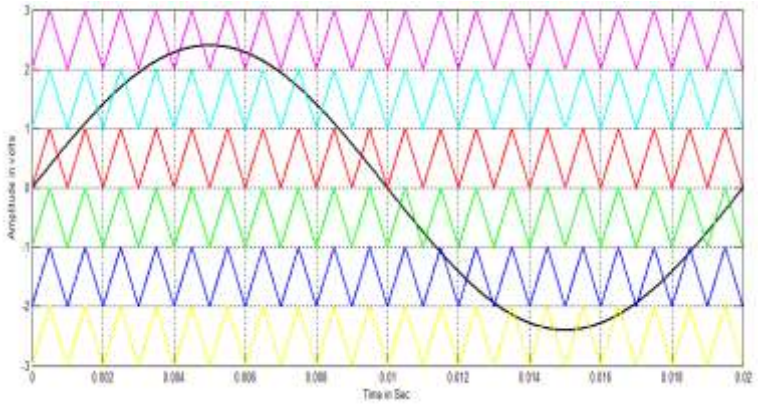

Figure 2. Multicarrier Arrangement for PDPWM Strategy

3.2. Alternate Phase Opposition Disposition Strategy

The six carriers are phase displaced from each other by 180 degrees alternately with identical frequency and peak to peak amplitude. Figure 3 Shows multicarrier arrangement for APOD method for m_a=0.8 and $m_{f=}$20.

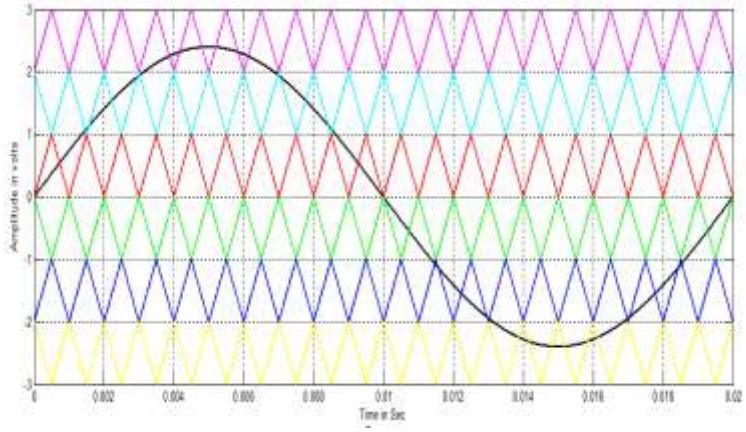

Figure 3. Multicarrier Arrangement for APODPWM Strategy

3.1 Carrier Overlapping Strategy

The COPWM strategy utilizes the control freedom degree of erect offsets among carriers. The principle of COPWM is to use a number of overlapping carriers with modulating signal. The six carriers disposed such that the bands they inhabit overlap each other. The overlapping magnitude among all carriers is A_c /2 in this work. Figure 4 shows the multicarrier arrangement for COPWM Strategy for $m_{a=}$0.8 and $m_{f=}$20.

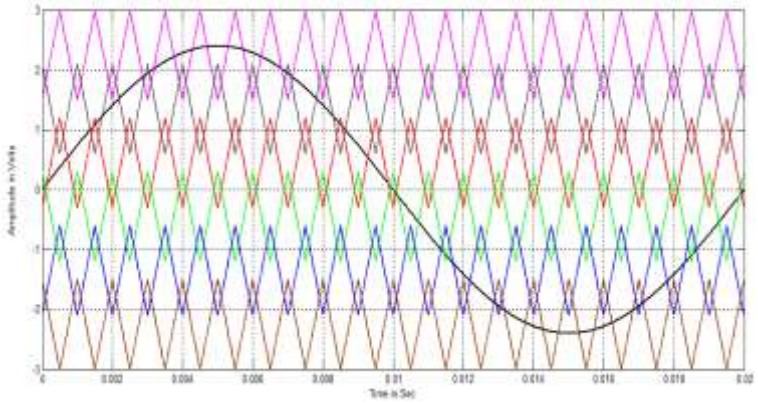

Figure 4. Multicarrier arrangement for COPWM strategy

4. SIMULATION RESULTS

The above symmetrical multilevel inverter is modeled in SIMULINK using power system block set. The gating signals are obtained by various PWM Strategy. Simulations are carried out for different modulation indices ranging from 0.7 to 1. The performance parameters like THD, V_{RMS}. Figures 5-10 display the simulated output voltage and their FFT plot with above strategies but for only one sample value of ma=0.8. Figure 10 & 11 explicites the graphical comparsion of all strategies.Figure 5 shows the seven level output voltage generated by PDPWM strategy and its FFT plot is shown in Figure 6. From Figure 6, it is observed that the PDPWM strategy produces significant 6^{th},8^{th},14^{th} and 20^{th} harmonic energy. Figure 7 shows the output voltage generated by APODPWM strategy and its FFT plot is shown in Figure 8. From Figure 8 it is observed that the APODPWM strategy produces significant 11^{th},13^{th},15^{th},17^{th} and 19^{th} harmonic energy. Figure 9 shows the seven level output voltage generated by COPWM strategy and its FFT plot is shown in Figure 10.From Figure 10 it is observed that the COPWM strategy produces significant 5^{th} ,11^{th} ,13^{th} ,15^{th} 17^{th} and 19^{th} harmonic energy.Table 2 indicates that % distortion factor is low compared with other strategies. The subsequent parameter values are taken for simulation: Vdc=100V, Resistive load – 10ohms, $f_{m=}$50 Hz, f_c=1000Hz.

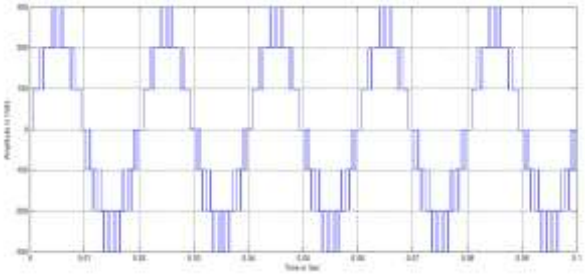

Figure 5. Simulated Output Voltage Generated by PDPWM

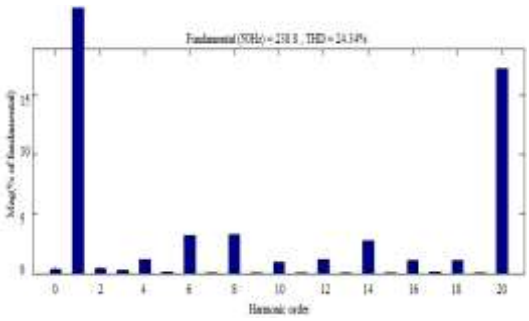

Figure 6. FFT Spectrum for PDPWM

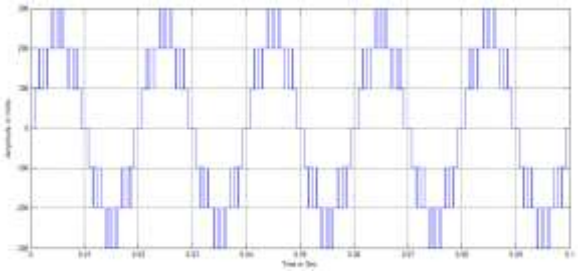

Figure 7. simulated output voltage generated by APODPWM

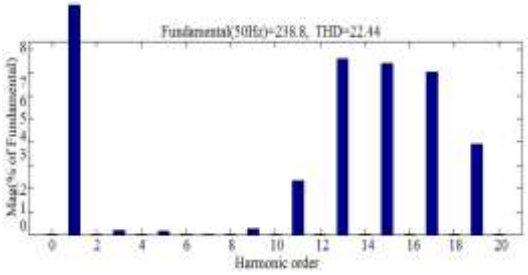

Figure 8. FFT spectrum for APODPWM

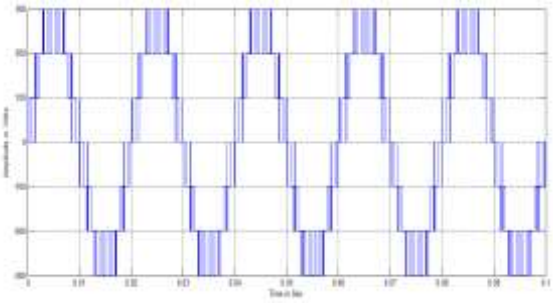

Figure 9. Simulated output voltage generated by COPWM

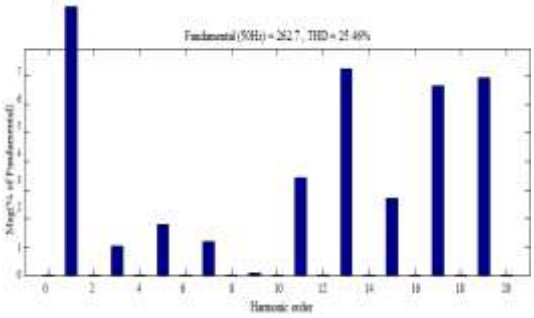

Figure 10. FFT spectrum for COPWM

Table 1. % THD for Different Modulation Indices

m_a	PD	APOD	CO
1.0	17.92	18.50	17.54
0.95	20.39	21.23	19.86
0.9	22.63	22.63	22.15
0.85	23.79	22.56	24.31
0.8	24.34	22.44	25.46
0.75	24.13	22.62	25.26
0.7	24.95	22.56	26.84

Table 2. % Distortion Factor for Different Modulation Indices

m_a	PD	APOD	CO
1	0.629	0.081	0.417
0.95	0.5256	0.0672	0.3546
0.9	0.4089	0.0742	0.2826
0.85	0.2424	0.0777	0.136
0.8	0.1754	0.0681	0.1491
0.75	0.2253	0.0826	0.2846
0.7	0.1462	0.0655	0.4525

Table 3. V_{RMS} for Different Modulation Indices

m_a	PD	APOD	CO
1.0	211.8	211.8	221.6
0.95	201.1	201.1	213.9
0.9	190.2	190.3	205.9
0.85	179.8	179.6	196.4
0.8	168.9	168.8	185.7
0.75	158.3	158.2	175.9
0.7	147.4	147.4	168.8

Table 4. Crest Factor for different modulation indices

m_a	PD	APOD	CO
1	1.414	1.414	1.418
0.95	1.414	1.414	1.417
0.9	1.414	1.414	1.415
0.85	1.414	1.414	1.418
0.8	1.414	1.414	1.427
0.75	1.508	1.414	1.424
0.7	1.414	1.414	1.392

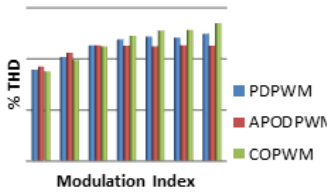

Figure 11. %THD comparison of various modulation indices

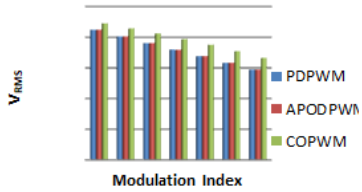

Figure 12. VRMS Comparison of Various Modulation Indices

5. HARDWARE RESULTS

This section presents the experimental work using Xilinx Spartan-3E XC3S100E FPGA system for symmetrical seven level inverter. Real time realization of these strategies using Spartan – 3 requires less time. The experimental studies are carried out to appraise the performance of the inverter. To verify the performance of the inverter design on Hardware, the VHDL code (Bit file) is downloaded into the desired FPGA device (Spartan 3 family XC3S100). The real time setup is shown in Figure 14. The results are taken from Digital Storage Oscilloscope (DSO) and analysed through power quality analyser. After suitably the scaling down the simulation values, due to laboratory constraints input voltage set as 45V, each DC source carries 15V and peak to peak output voltage experimentally is 90V.

Figure 14. Hardware Setup of Symmetrical Multilevel Inverter

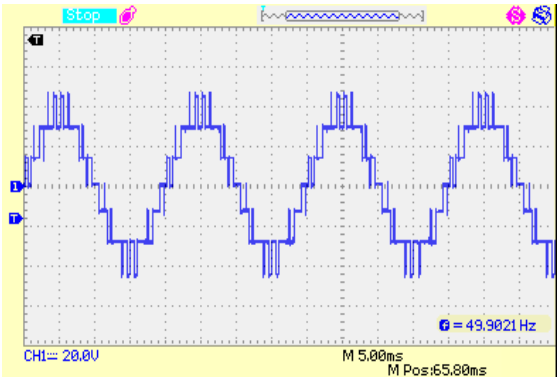

Figure 15 Hardware Output voltage of generated by PDPWM

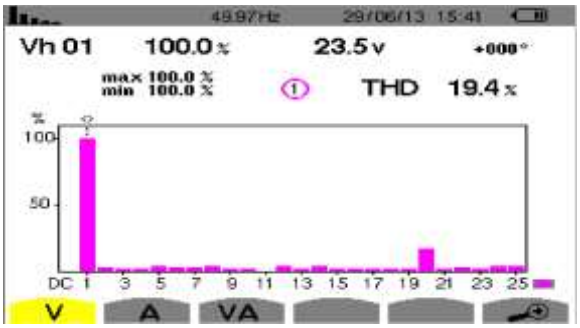

Figure 16. FFT spectrum for PDPWM

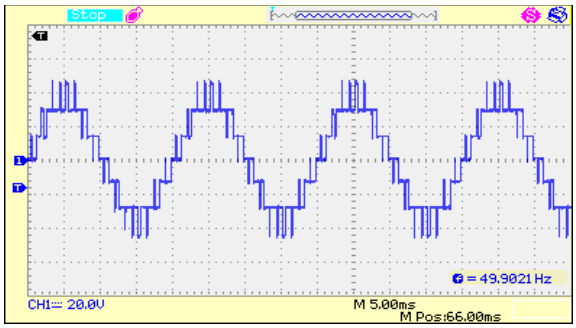

Figure 17. Hardware output voltage generated by APODPWM

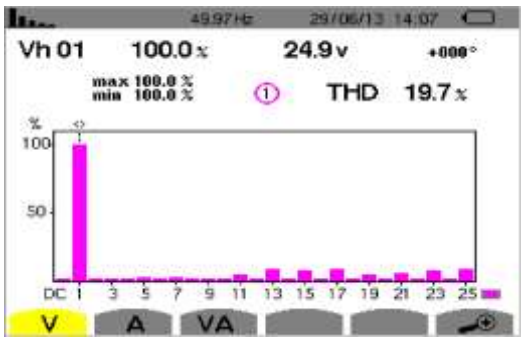

Figure 18. FFT spectrum for APODPWM

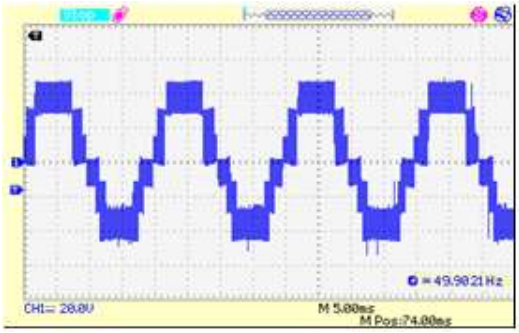

Figure 19. Hardware output voltage generated by COPWM

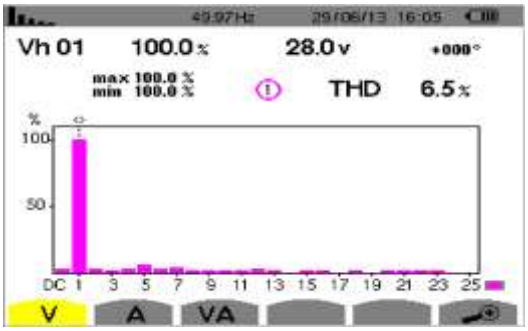

Figure 20. FFT spectrum for COPWM

Table 5. % THD for different modulation indices

m_a	PD	APOD	**CO**
1.0	14.7	15.5	6.0
0.95	17.1	15.8	6.0
0.9	19.1	18.6	6.1
0.85	20.1	19.7	6.2
0.8	19.4	19.7	6.5
0.75	19.5	21.3	6.6
0.7	19.1	21.0	6.8

Table 6. % Distortion Factor for different modulation indices

m_a	PD	APOD	CO
1	14.6	15.4	6.5
0.95	17.1	17.9	6.7
0.9	18.7	19.4	6.3
0.85	19.9	19.9	6.6
0.8	19.4	19.7	6.4
0.75	19.8	21.4	7.2
0.7	20	18.1	6.9

Table 7. V_{RMS} for different modulation indices

m_a	PD	APOD	CO
1.0	31.8	31.7	33.5
0.95	30.3	30.2	32.3
0.9	28.6	28.6	30.7
0.85	25.5	27.0	29.6
0.8	23.5	24.9	28.0
0.75	22.4	23.8	26.7
0.7	22.1	22.4	25.0

Table 8. Crest Factor for different modulation indices

m_a	PD	APOD	CO
1	1.41	1.4	1.31
0.95	1.48	1.49	1.36
0.9	1.56	1.56	1.4
0.85	1.64	1.64	1.45
0.8	1.75	1.74	1.52
0.75	1.86	1.86	1.58
0.7	1.94	1.78	1.65

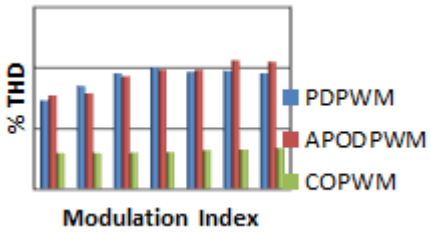

Figure 21. %THD comparison of various modulation indices

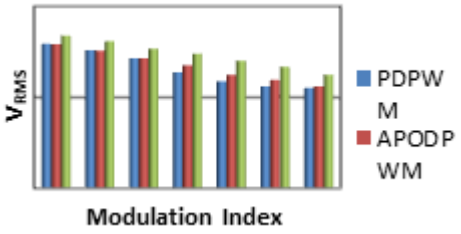

Figure 22. V_{RMS} comparison of various modulation indices

6. CONCLUSION

In this paper, the various modulation strategies for reduced switch seven level Symmetrical Inverter have been discussed. The various performance parameters like %THD ,V_{RMS} ,Distortion Factor and Crest Factor have been analysed and evaluated. It is observed that the Carrier Overlapping PWM provides least %THD and Distortion factor for all m_a and provides maximum RMS voltages when compared to other two strategies. At the same time APOD strategy provides nominal crest factor. The simulation results were closely matched with experimental results.

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