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A New Multilevel Inverter Structure For High-Power Applications using Multi-carrier PWM Switching Strategy

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ABSTRACT

In recent, several numbers of multilevel inverter structures have been introduced that the numbers of circuit devices have been reduced. This paper introduces a new structure for multilevel inverter which can be used in high-power applications. The proposed topology is based on cascaded connection of basic units. This topology consists of minimum number of circuit components such as IGBT, gate driver circuit and antiparallel diode. For proposed topology, two methods are presented for determination of dc voltage sources values. Multi-carrier PWM method for 25-level proposed topology is used. Verification of the analytical results is done using MATLAB simulation.

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1. INTRODUCTION

Multilevel inverters in comparison with two level converter can generate output voltage waveform with lower value of the total harmonic distortions (THD) and the value of voltage stress on circuit devices is low [1, 2]. Multilevel inverters are used in more applications such as Electric/Hybrid electric vehicles, renewable energy sources, FACTS devices and so on [3-5]. In general, there are three kinds of conventional multilevel inverter structures which have been named as follows:

- Diode-Clamped Multilevel Inverter [6].
- Flying-capacitors Multilevel Inverter [7].
- Cascade Multilevel Inverter [8].

The most important topology among classical multilevel inverters is cascade converter with separated dc sources [9, 10]. Cascade inverter requires the least number of components when compared to flying capacitor and diode clamped inverters. The cascaded inverter consists of a number of H-bridge inverter units with separate dc source for each unit and it is connected in cascade or series [11, 12].

Cascade inverter is classified into two types which are called symmetric and asymmetric configurations. The symmetric configuration uses the dc voltage sources with the same magnitudes. In the asymmetric configuration, the values of the dc sources are non-equal. Asymmetric configuration can produce many numbers of output voltage levels in comparison with symmetric configuration [13, 14]. The symmetric configuration has the advantage of modularity that makes them simple to design and extend. But, the number of power electronic switches increases.

Some applications need multilevel inverter topologies with capability of unidirectional power flow such as photovoltaic systems or fuel cells. For this aim, a new unidirectional multilevel inverter topology has

been proposed in [4]. The main disadvantage of this topology is that the switches of full-bridge inverter must withstand the sum of the values of DC sources. It leads to the limitation in high-power applications.

Several modulation technique have been improved for multilevel inverters such as sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), selective harmonic elimination (SHE-PWM), fundamental frequency switching and so on [15]-[19]. This paper focuses on multi-carrier-PWM modulation strategy for trigger the power switches for controlling the voltage levels generated on the output.

This paper presents a new topology for multilevel inverter which needs minimum number of power electronic elements.

2. PROPOSED TOPOLOGY

Figure 1 shows the basic unit structure for proposed multilevel inverter.

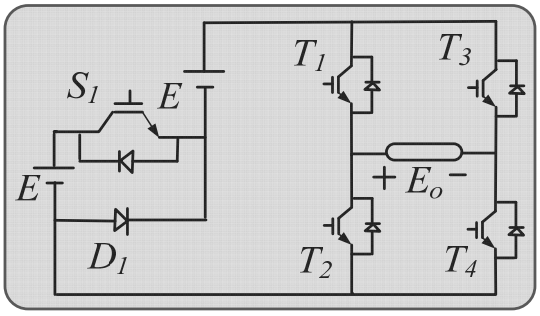

Figure 1. Basic unit structure for proposed multilevel inverter.

This basic unit can generate five levels at the output voltage $(0, E, -E, 2E, -2E)$. Table I shows the switching states of proposed basic unit for generation five levels at the output voltage waveform.

Table I. Switching States of Proposed Basic Unit.

State	*Switches*					*Output voltage*
	S_1	T_1	T_2	T_3	T_4	
1	0	1	0	1	0	*0*
2	0	1	0	0	1	*E*
3	0	0	1	1	0	*-E*
4	1	1	0	0	1	*2E*
5	1	0	1	1	0	*-2E*

To produce an output voltage waveform with high quality and lower value of harmonic distortions, the number of output voltage levels must be increased. Therefore, a cascade topology based on series connection of basic units is proposed. Figure 2 shows the proposed cascade multilevel inverter. The output voltage of the proposed cascade inverter is obtained by:

$$E_o = E_{o1} + E_{o2} + ... + E_{on} \quad (1)$$

The number of used IGBTs in proposed cascade structure is given by the following relationship:

$$N_{IGBTs} = 5n \quad (2)$$

In this equation, N_{IGBT} represents the number of used IGBTs. In this structure, the dc voltage sources magnitudes of each basic unit are the same. For proposed cascade inverter two methods are presented to generate all levels (odd and even) in the output voltage.

2.1. First Method

In this method, the values of dc sources are the same. In the other words, we have

$$E_1 = E_2 = ... = E_n \tag{3}$$

Because the values of dc sources are the same, this topology is named symmetric topology. For this method, the number of output voltage levels is calculated by the following equation:

$$N_{level} = 4n + 1 \tag{4}$$

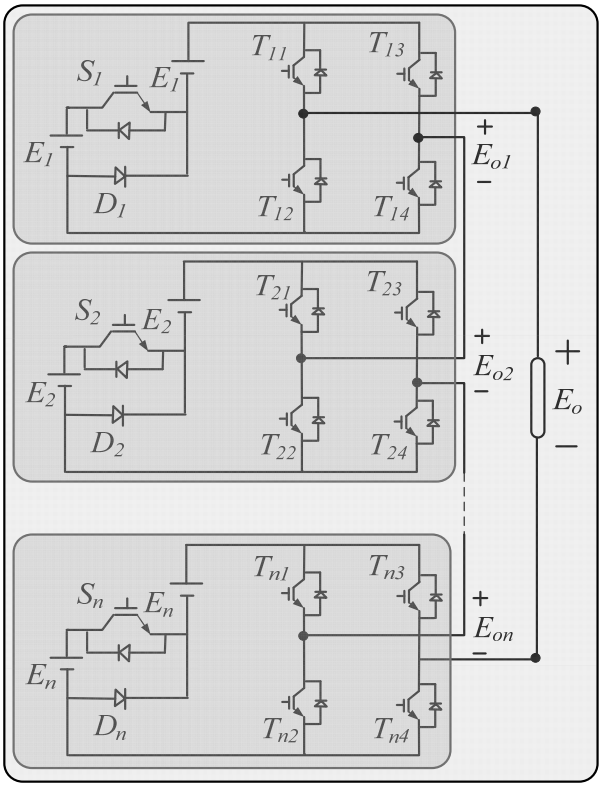

Figure 2. Proposed cascade multilevel inverter structure

Where n represents the number of basic units in the proposed cascade structure. From (2) and (4), we have

$$N_{level} = \frac{4}{5} N_{IGBT} + 1 \tag{5}$$

2.2. Second Method

In this method, the magnitudes of dc voltage sources are obtained by:

$$E_1 = E \tag{6}$$

$$E_m = 5^{m-1} \times E \qquad m = 2,3,\ldots n \tag{7}$$

Using this method, the number of output voltage levels is calculated by:

$$N_{level} = 5^n \tag{8}$$

Using (2) and (8), the relation between the number of output voltage levels and IGBTs will be:

$$N_{level} = 5^{\frac{N_{IGBT}}{5}} \quad (9)$$

In this method, the magnitudes of dc sources are non-equal. Hence, this method is named asymmetric configuration. It is noticeable that Instead of dc voltage sources, we can use capacitors, fuel cells and so on. The voltage stress of switches depends on the sum of all dc sources which connected to special full-bridge inverter and their values are very low. Therefore, this topology can be used in high-power applications. Figure 3 shows the structure of proposed multilevel inverter topology in [4]. As shown in this figure, the switches of full-bridge inverter must withstand high-voltage. Then, this structure is not suitable for high-power applications.

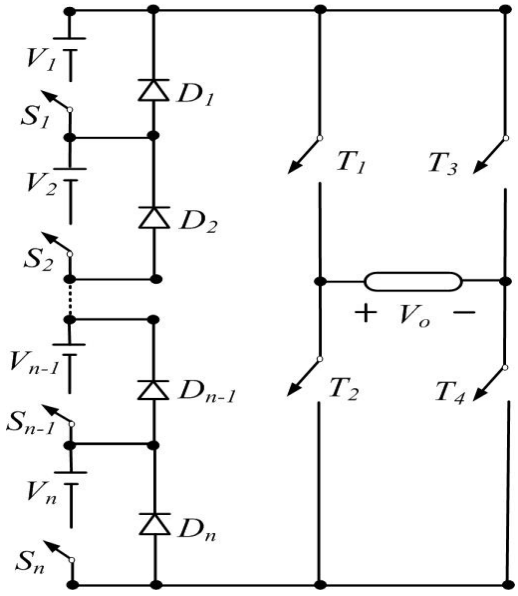

Figure 3. The structure of proposed multilevel inverter topology in [4]

3. MULTI-CARRIER PWM STRATEGY

The harmonics in the output voltage of power electronic converters can be reduced using PWM switching techniques. The widely used multi-carrier PWM methods are known as Phase Shifted (PS), Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposite Disposition (APOD), Hybrid (HD) and Phase Shift (PS). For this topology, phase opposite disposition (POD) multi-carrier PWM method is utilized. POD technique employs a number of carriers (*m-1*) for an m-level phase waveform which are all in-phase above and below the zero reference. The carriers are defined with the same frequency (F_c) and amplitude (A_c) The amplitude of the modulator is denoted as (A_m) and the frequency (F_m). In multilevel converters, the amplitude modulation index (M_a), and the frequency ratio (M_f) are given by (10) and (11), respectively:

$$M_a = \frac{A_m}{(m-1)A_c} \quad (10)$$

$$M_f = \frac{F_m}{F_c} \quad (11)$$

The switching functions of proposed inverter are then given by the use of logical AND, OR, NOT gates.

4. SIMULATION REULTS

In order to validate the proposed inverter, computer simulation using MATLAB-Simulink has been created. The simulation studies are carried out for 25-level asymmetric multilevel inverter. The total harmonic distortion (THD) evaluates the quantity of harmonic contents in the output waveform and is a popular performance index for power converters. The asymmetric multilevel inverter shown in Figure 3 is adjusted to produce a 50-Hz, 25-level staircase waveform. The parameters selected for testing are (a) an inductive load of *50mH* (b) a resistive load of 50Ω. The values of voltage sources are $E_1 = 12.5V$ and $E_2 = 62.5V$.

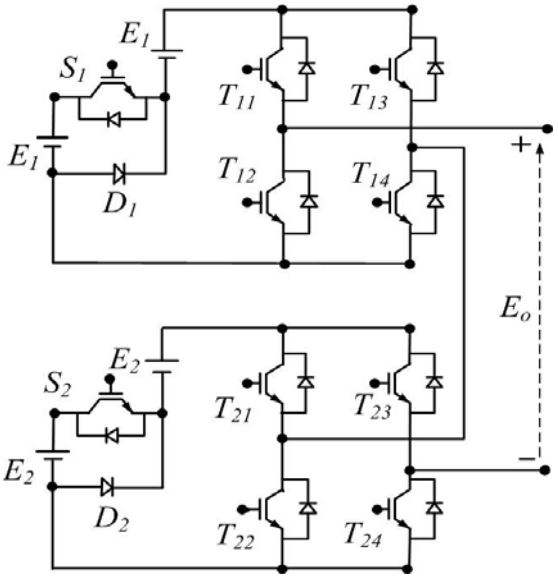

Figure 4. Proposed 25-level cascade inverter

Table II shows the switching states of proposed 25-level cascade inverter.

Table II. Switches states for 25-level cascade topology.

State	Switches State										Output Voltage(V)
	S_{11}	S_{21}	T_{11}	T_{12}	T_{13}	T_{14}	T_{21}	T_{22}	T_{23}	T_{24}	
1	1	1	1	0	0	1	1	0	0	1	150
2	0	1	1	0	0	1	1	0	0	1	137. 5
3	0	1	1	1	0	0	1	0	0	1	125
…….	….	….	….	….	….	….	….	….	….	….	….
12	0	0	1	0	0	1	1	1	0	0	12.5
13	0	0	1	1	0	0	1	1	0	0	0
14	0	0	0	1	1	0	1	1	0	0	-12.5
……..	….	….	….	….	….	….	….	….	…..	…..	….
23	0	1	1	1	0	0	0	1	1	0	-125
24	0	1	0	1	1	0	0	1	1	0	-137.5
25	1	1	0	1	1	0	0	1	1	0	-150

Figure 5 shows the carriers and the reference signals for a 25- level PWM using POD technique with $M_a = 1$, $M_f = 48$ and carrier frequency 2400 Hz.

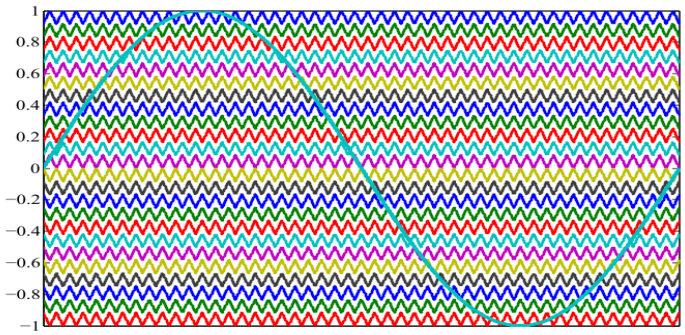

Figure 5. The carriers and the reference signals for a 25- level converter using POD technique

The output voltage and current waveforms and their corresponding Fourier spectrums are shown in Figure 6. THD values of this output voltage and current based on simulation results are %5.57 and %0. 83. To generate a desired output with best quality of the waveform, the number of the voltage levels should be increased.

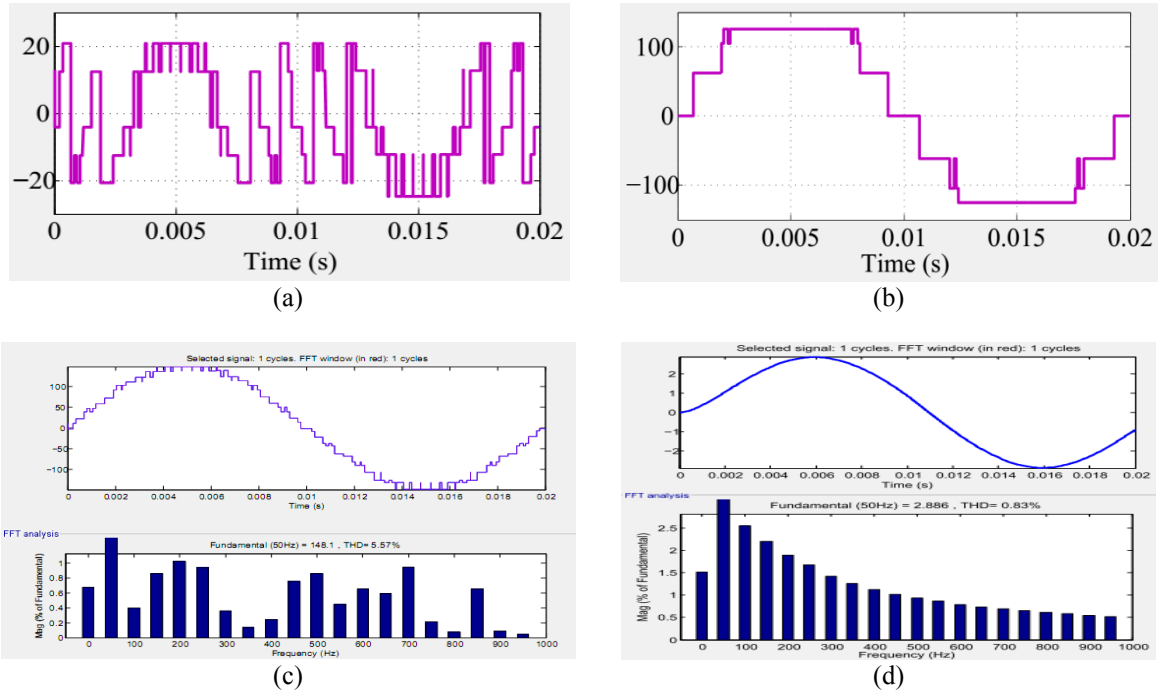

Figure 6. (a) Simulated output voltage of the first stage
(b) Simulated output voltage of the second stage
(c) Simulated output voltage and corresponding Fourier spectrum (THD=5.57%)
(d) Simulated output current and corresponding Fourier spectrum (THD=0.083%)

5. CONCLUSION

New symmetric, asymmetric cascade multilevel inverter topologies were proposed in this paper. New algorithms for determination of dc voltage source magnitudes in the proposed cascade topology were presented. This technique provides more voltage levels without increasing number of power electronic components. Multi-carrier PWM method is applied to the new topology to trigger the power switches for controlling the voltage levels generated on the output. It was shown that the presented topology can be used in high-power applications. Through simulations it is seen that proposed multilevel converter topology generates lower value of harmonic components of load voltage and current.

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