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Analysis of Various Carriers Overlapping PWM Strategies for a Single Phase Ternary Multilevel Inverter

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ABSTRACT

Multilevel inverters are used in power conversion system due to improved voltage and current waveforms. This paper presents the comparison of various carrier overlapping pulse width modulation (COPWM) strategies for the three phase cascaded multi level inverter (CMLI). Various new schemes adopting the constant switching frequency and also variable switching frequency multicarrier control freedom degree combination concepts are developed and simulated for the chosen three phase CMLI. A single phase CMLI is controlled in this paper with sinusoidal PWM (SPWM) reference along with carrier overlapping (CO) techniques and simulation is performed using MATLAB-SIMULINK. The variation of fundamental RMS output voltage and total harmonic distortion is observed for various carrier overlapping techniques. Among the various equal amplitude and unequal amplitude carriers carrier overlapping techniques such as COPWM-A, COPWM-B and COPWM-C, It is observed from Table 4 that all PWM method provides output with relative low distortion for equal amplitude carriers. If equal voltage sources are chosen then the THD will be less in the case of unequal amplitude carriers. But for the unequal voltage sources the THD is more in the case of unequal amplitude carriers. It is observed from simulation results that (Table-5) almost in all the strategies unequal amplitude carriers gives more fundamental RMS values compared to equal amplitude carriers. It is seen from table 6 that peak voltage is more in the case of unequal amplitude carriers compared to equal amplitude carriers. It is observed from the Table 7 that dc components are less in both equal and unequal amplitude carriers.

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1. INTRODUCTION

Multi-level inverters play a key role in today's microgrids with renewable energy sources. It is a power electronic device that is used for high voltage and high power applications, with the added advantages of low switching stress and lower total harmonic distortion (THD), hence reducing the size and bulk of the passive filters. It gives the output current waveform which is nearly sinusoidal in nature. Jamaludin et al [1] suggested a multilevel voltage source inverter with optimised usage of bidirectional switches. Manjunatha and Anand [2] proposed a multilevel DC Link Inverter with reduced switches and batteries. Pharne and Bhosale [3] made a review on various multilevel inverter topology. Prasad et al [4] made a comparsion on different topologiesof cascaded h-bridge multi-level inverters. Lakshmi et al [5] developed a Cascaded seven level inverter with reduced number of switches using level shifting PWM technique. Najafi et al [6]

evaluated a new design of a multilevel inverter topology. Ebrahimi et al [7] introduced a new multilevel converter topology with reduced number. Roshankumar et al [8] deals a five-level inverter topology with single-DC supply by cascading a flying capacitor inverter. James et al [9] proposed a multilevel inverter with reduced number of switches. Rahilal et al [10] evaluated a new 81 level inverter with reduced number of switches. Bayat and Babaei [11] introduced a new cascaded multilevel inverter with reduced number of switches. Nedumgatt et al [12] also introduced a multilevel inverter with reduced number of switches. Ho-Sun et al [13] proposed a multi-level inverter capable of power factor control with dc link switches. Adam et al [14] decribes a quasi-two-level and three-level operation of a diode-clamped multilevel inverter using space vector modulation. Gupta and Jain [15] made a topology for multilevel inverters to attain maximum number of levels from given DC sources. Lakshmi Ganesh and Chandra Rao [16] discussed the performance of symmetrical and asymmetrical multilevel inverters. Ebrahimi et al [17] introduced a new topology of cascaded multilevel converters with reduced number of switch count for high-voltage applications. Caballero et al [18] suggested a symmetrical hybrid multilevel inverter concept based on multi-state switching cells. Suroso and Toshihiko Noguchi [19] introduced a multilevel voltage-source inverter using h-bridge and two-level power modules with a single power source. Balamurugan [20] made a comparision between simulation and dSPACE based implementation of various PWM strategies for a new H-type FCMLI topology. Balamurugan [21] introduced a nine level cascaded multi level inverter using embedded and flip flops. The above papers made a deep literature surevy on various multilevel invereters and its topologies.

2. TERNARY INVERTER

Figure 1 shows a circuit configuration of a cascaded H-bridge multilevel inverter employing trinary dc input source. It looks like a traditional cascaded H-bridge multilevel inverter except input dc sources. By using Vdc and 3Vdc, it can synthesize five output levels; -3Vdc, -Vdc, 0, Vdc, 3Vdc. The lower inverter generates a fundamental output voltage with three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge, and it is given as

$$\mathbf{V}_{out}=V_{HB1}+V_{HB2} \quad (1)$$

Table 1 and 2 shows the different switching states for the ternary inverter and comparison between symmetrical and asymmetrical inverters. In the proposed circuit topology, if *n* number of H-bridge module has independent DC sources in sequence of the power of 3, an expected output voltage level is given as

$$V_n=3^n,\ n=1,2,3 \quad (2)$$

Table 1. Switching States for Ternary Output

$\mathbf{V_{out}}$	$\mathbf{S_{11}}$	$\mathbf{S_{12}}$	$\mathbf{S_{13}}$	$\mathbf{S_{14}}$	$\mathbf{S_{21}}$	$\mathbf{S_{22}}$	$\mathbf{S_{23}}$	$\mathbf{S_{24}}$
$\mathbf{4V_{dc}}$	1	0	0	1	1	0	0	1
$\mathbf{3V_{dc}}$	0	1	0	1	1	0	0	1
$\mathbf{2V_{dc}}$	0	1	1	0	1	0	0	1
$\mathbf{V_{dc}}$	1	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
$\mathbf{-V_{dc}}$	0	1	1	0	0	1	0	1
$\mathbf{-2V_{dc}}$	1	0	0	1	0	1	1	0
$\mathbf{-3V_{dc}}$	0	1	0	1	0	1	1	0
$\mathbf{-4V_{dc}}$	0	1	1	0	0	1	1	0

Table 2. Comparison between Symmetrical and Asymmetrical Inverters

Comparison	Symmetrical inverter	Asymmetrical inverter	
		Binary	Ternary
Levels	2N+1	2^{N+1}-1	3^N
DC sources	N	N	N
Switches	4N	4N	4N

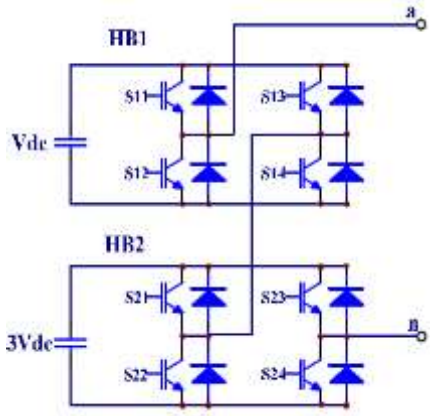

Figure 1. Power circuit for single phase nine level cascaded multilevel inverter

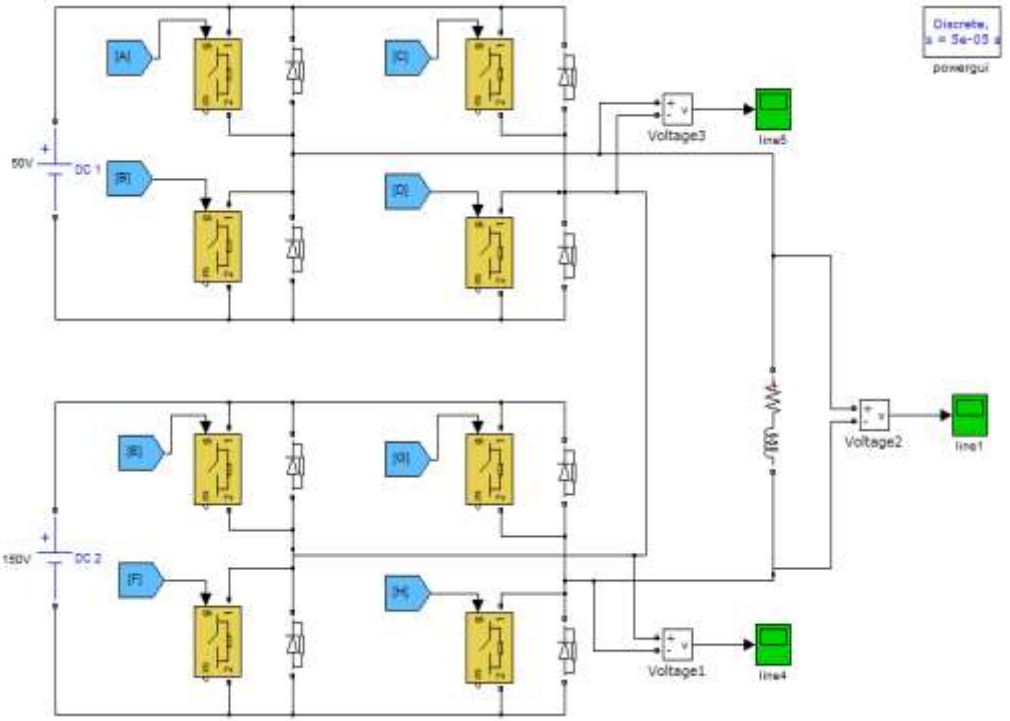

Figure 2. Sample PWM generation logic model developed using SIMULINK for COPWM-A technique

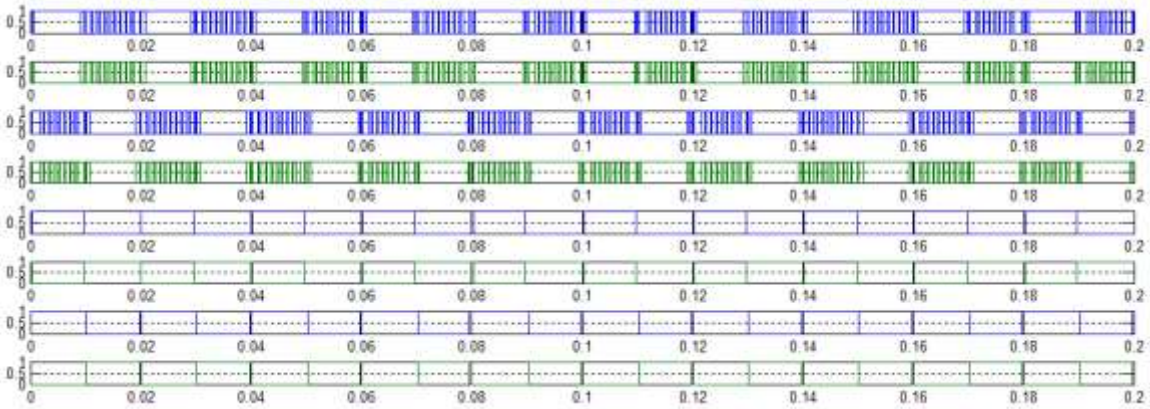

Figure 3. PWM signal pattern for various switches

3. MODULATION STRATEGIES

Several CFDs exist in multi-carrier PWM strategies for MLIs. These strategies have more than one carrier option that can be triangular, saw tooth, a new function etc. As far as the particular carrier signals are concerned, there are multiple CFDs including function, frequency, amplitude, phase of each carrier and offset between carriers. Although multilevel inverter offers several advantages, the control strategies of MLI are quite challenging due to the complexity to cater the transitions between the voltage levels (or steps). A number of modulation strategies are used in multilevel power conversion applications. In this proposed topology two methods are used.

1. Equal amplitude carriers
2. Un equal amplitude carriers (or) variable amplitude carriers (VAC)

3.1. Equal amplitude carriers (EAC)

In this method, all the triangular carriers used will have the same amplitude. The PWM methods used are COPWM-A, COPWM-B AND COPWM-C WITH sine, THI, trapezoidal and stepped wave references. Figure. 4 to 6 shows the sample carrier arrangement, output voltage and FFT plot for COPWM-A strategy with sine reference (m_a=0.8 and m_f=20). Where m_a and m_f are the amplitude and frequency modulation index.

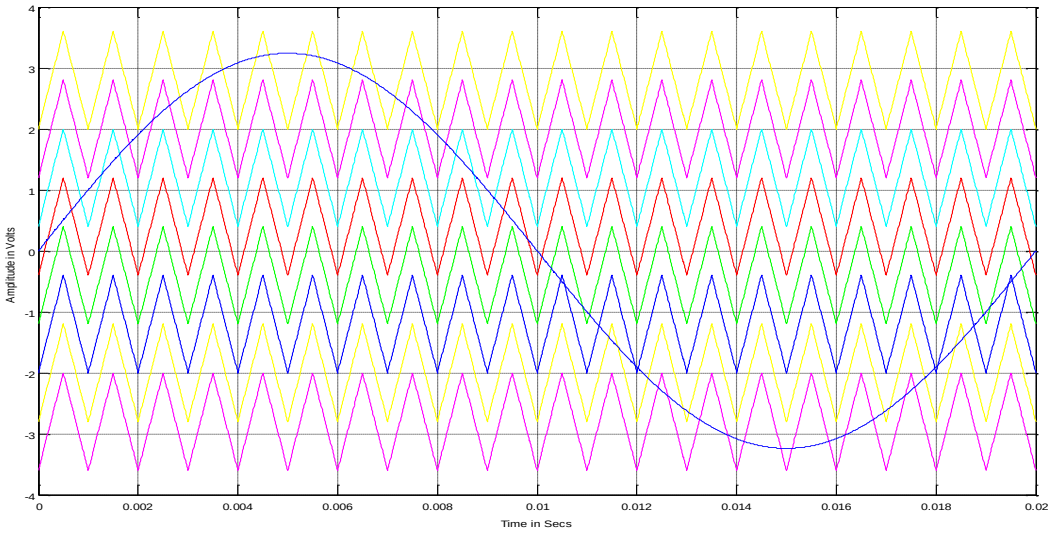

Figure 4. Sample carrier arrangement for equal amplitude carriers with COPWM-A strategy (sine reference for m_a=0.8, $m_{f=}$20)

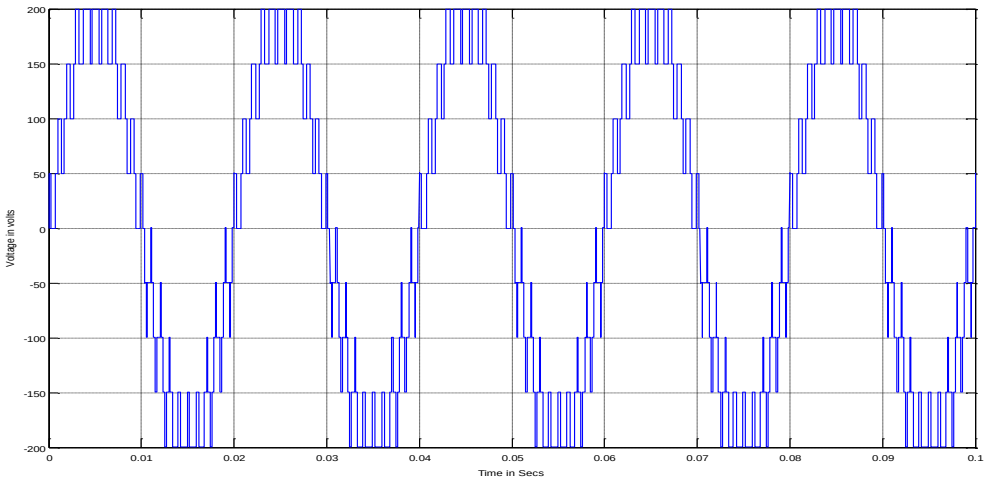

Figure 5. Sample output voltage of five level inverter based on equal amplitude carriers with COPWM-A strategy (sine reference for m_a=0.8, $m_{f=}$20)

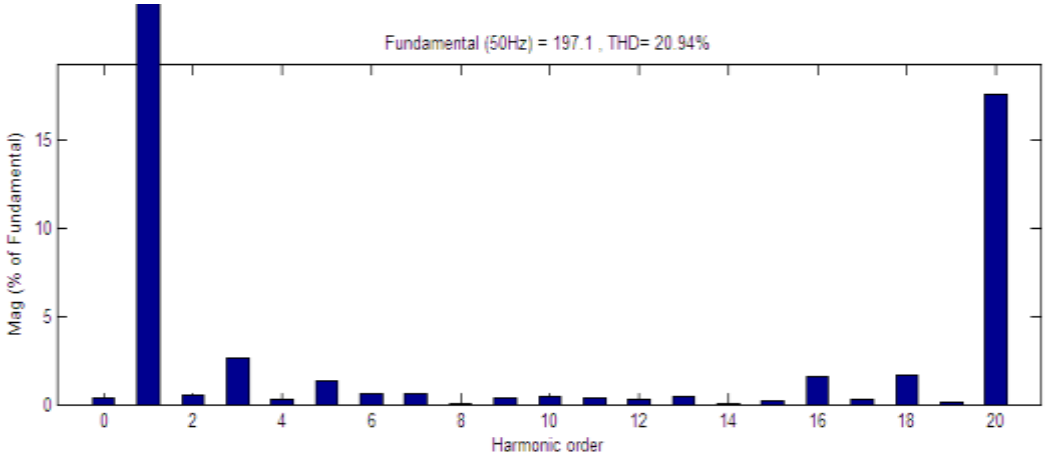

Figure 6. Sample THD plot for five level output voltage based on equal amplitude carriers with COPWM-A strategy (sine reference for m_a=0.8, m_f=20)

3.2. Un equal amplitude carriers (UEAC) (or) variable amplitude carriers (VAC)

In this method, all the triangular carriers used will not have the same amplitude. The PWM methods used are UEAPD (Un Equal Amplitude Phase Disposition) PWM, UEAPODPWM, UEAAPODPWM, UEACOPWM, UEAPSPWM and UEAVFPWM with sine, THI, trapezoidal, TAR and stepped wave references. Figure 7 to 9 shows the sample carrier arrangement, output voltage and FFT plot for COPWM-A strategy with sine reference (m_a=0.8 and m_f=20).
where:

$$m_a = \frac{A_m}{A_c} \quad (3)$$

$$m_f = \frac{f_c}{f_m} \quad (4)$$

Where :
m_f : Frequency modulation index
ma : Amplitude modulation index
A_m : Amplitude of modulating signal
A_c : Amplitude of carrier signal
f_c : Frequency of carrier signal
f_m : Frequency of modulationg signal

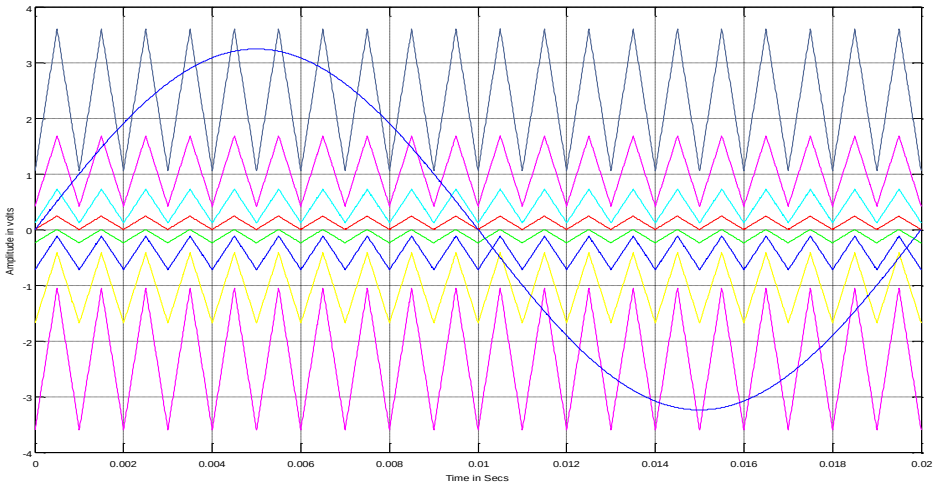

Figure 7. Sample carrier arrangement for equal amplitude carriers with COPWM-A Strategy (Sine Reference for m_a=0.8, m_f=20)

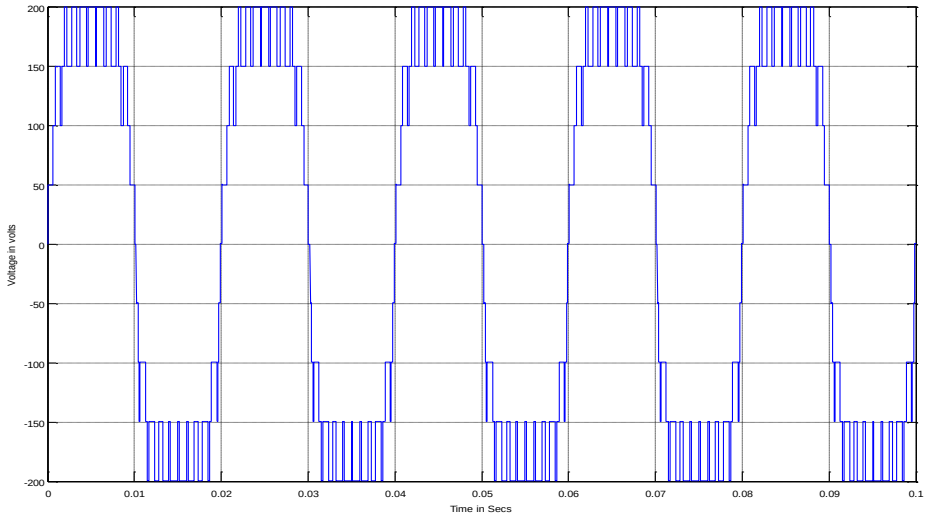

Figure 8. Sample output voltage of five level inverter based on equal amplitude carriers with COPWM-A strategy (sine reference for m_a=0.8 , $m_{f=}$20)

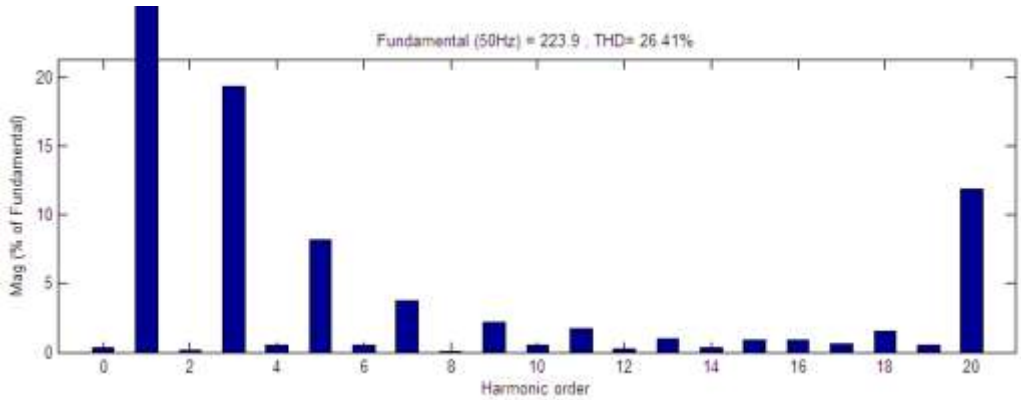

Figure 9. Sample THD plot for five level output voltage based on equal amplitude carriers with COPWM-A strategy (sine reference for m_a=0.8 , $m_{f=}$20)

4. CARRIER OVERLAPPING PWM STRATEGIES

The COPWM method utilizes the CFD of vertical offsets among carriers. The principle of COPWM is to use several overlapping carriers with single modulating signal. For an m-level inverter, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other. The overlapping vertical distance between each carrier is $A_c/2$ in this work. The reference wave has the amplitude A_m and frequency f_m and it is centered in the middle of the carrier signals. Within this COPWM strategy, combination of varied vertical and/or horizontal offsets are adopted to get different species such as COPWM-A, COPWM-B and COPWM - C.

The amplitude modulation index $$m_a = \frac{A_m}{\left(\frac{m}{4}\right)A_c}$$

Actually COPWM-B and COPWM-C can be looked on as a second control freedom degree change besides offset in vertical: the carriers have horizontal phase shift from COPWM - A. This formula is applicable only for the equal amplitude carriers.

4.1. COPWM-A strategy

The vertical offset of carriers for chosen five level inverter can be illustrated in Figure 10. It can be seen that the four carriers are overlapped with other and the reference sine wave is placed at the middle of the four carriers.

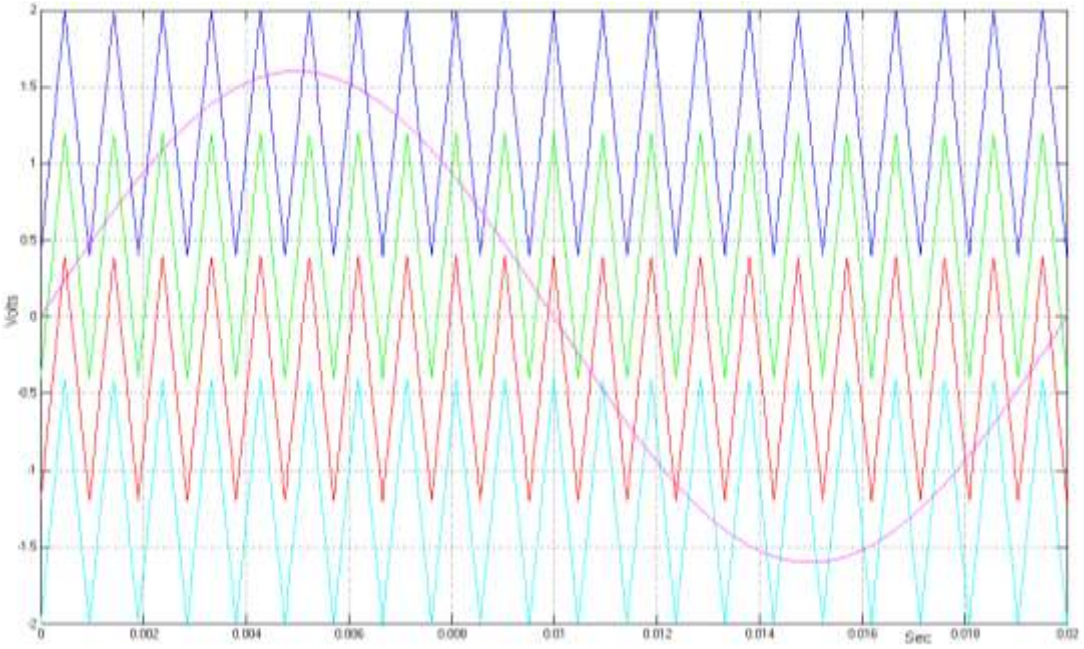

Figure. 10 Carrier arrangement for COPWM-A strategy (m_a=0.8, m_f=21)

4.2. COPWM-B strategy

Carriers for chosen five level inverter with COPWM-B strategy are shown in Figure 11. It can be seen that they are divided equally into two groups according to the positive/negative average levels. In this strategy, the two groups are opposite in phase with each other while keeping in phase within the group.

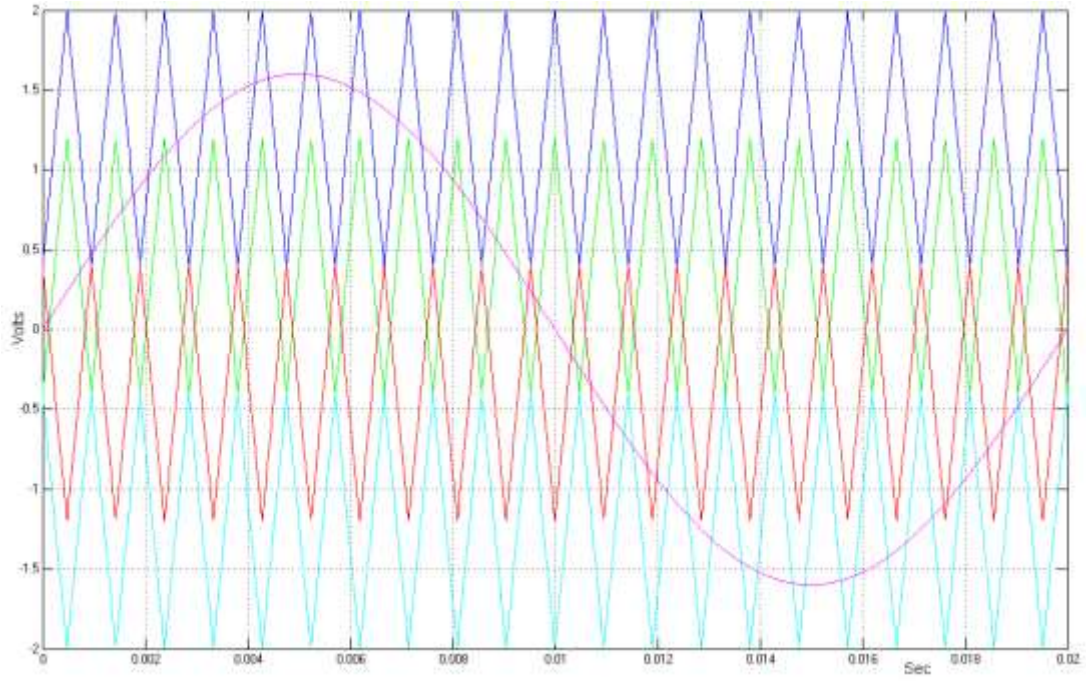

Figure. 11 Carrier arrangement for COPWM-B strategy (m_a=0.8, m_f=21)

4.3. COPWM-C strategy

Carriers for chosen five level inverter with COPWM-C strategy are shown in Figure 12. In this strategy, carriers invert their phase in turns from the previous one. It may be identified as PWM with amplitude overlapped and neighbouring phase interleaved carriers.

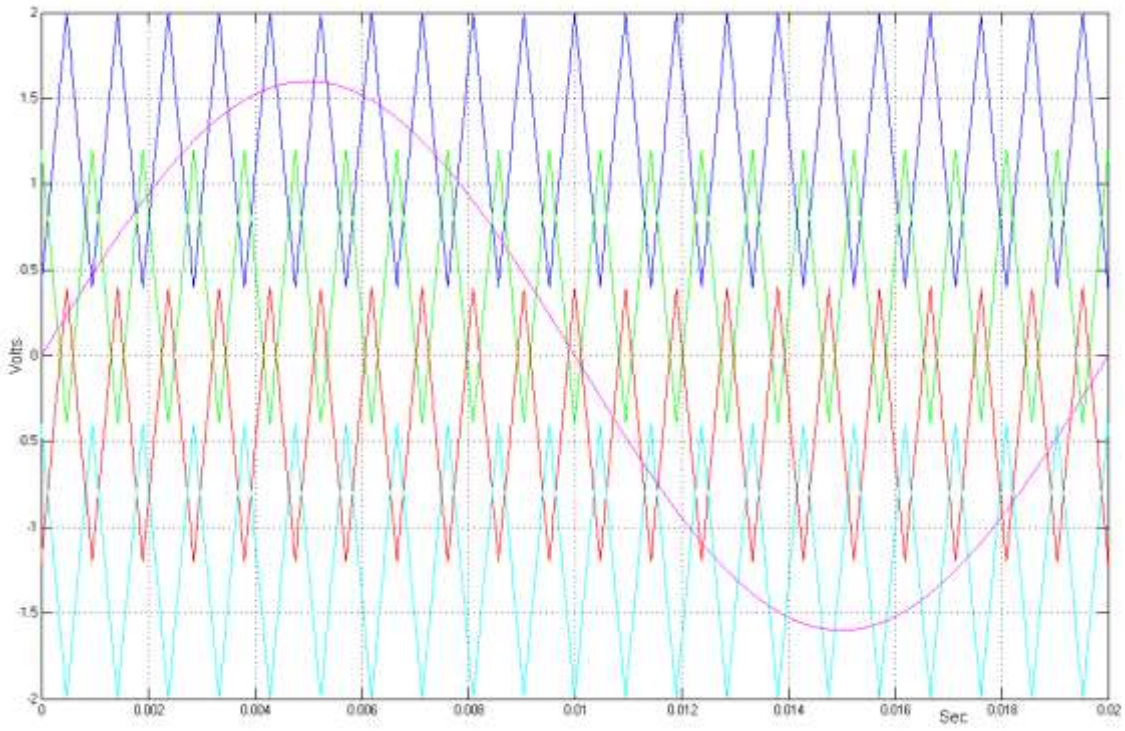

Figure. 12 Carrier arrangement for COPWM-C strategy (m_a=0.8, m_f=21)

5. SIMULATION RESULTS

The following parameters are used for the simulation V_{dc1}=50V, V_{dc2}=150V, R (Resistance)=100 ohms, , A_c (Amplitude of the carrier signal)=1,2,3 and 4 (EA), 0.25, 0.5, 1 and 2 (UEA), A_m (Amplitude of the modulating signal=2, f_c (frequency of the carrier signal)=1000 Hz and f_m (frequency of the modulating signal)=50 Hz. Table 3 (a) and (b) shows the circuit parameters choosen for simulation and comparison of various output levels between Equal Amplitude (EA) and Unequal Amplitude (UEA) carrries. Tables 4, 5, 6 and 7 displays the %THD, Vrms, Vpeak and DC component for equal and unequal amplitude cariers with various references and various COPWM strategies.

Table 3(a). Circuit Parameters for Various Components Used for Simulation

Parameters	MOSFET Switch	Feedback diode
R_{on} (Resistance)	0.001 Ω	0.001 Ω
L_{on} (Internal diode inductance)	1e $^{-6}$ H	0 H
R_d (Internal diode resistance)	0.001 Ω	-
V_f (Internal forward voltage)	0 V	0.8 V
I_c (Initial current)	0 A	0 A
R_s (Snubber resistance)	10 Ω	10 Ω
C_s (Snubber capacitance)	INF	INF

Table 3 (b). Comparison of Various Output Levels between EA Carriers and UEA Carriers

Ref.	m_a	PWM techniques	
		PD	UEAPD
Sine, THI, 60 degree and Stepped wave reference	1	9-level	9-level
	0.9		
	0.8		
	0.7	7-level	
	0.6		
	0.5		7-level
	0.4	5-level	
	0.3		
	0.2		5-level
	0.1	3-level	
	>0 to < 0.09		3-level

Table 4. %THD for Nine Level Output Voltage Based on Equal Amplitude and Unequal Amplitude Carriers with Various Modulation Indices

Ref.	m_a	% THD for 9-level inverter					
		COPWM-A		COPWM-B		COPWM-C	
		EA	UEA	EA	UEA	EA	UEA
Sine reference	1	18.69	25.69	18.73	25.48	16.98	22.68
	0.9	20.94	26.41	20.46	25.63	19.78	22.91
	0.8	24.23	26.44	23.35	25.91	25.78	23.88
	0.7	7-level	26.57	7-level	26.48	7-level	23.11
	0.6		25.71		25.25		22.75
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
THI reference	1	26.06	33.10	25.05	32.31	30.25	34.54
	0.9	28.23	34.71	27.98	34.42	30.28	36.62
	0.8	29.67	34.11	29.18	33.47	30.22	34.49
	0.7	7-level	34.15	7-level	33.01	7-level	32.05
	0.6		33.41		32.87		30.10
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
Trapezoidal reference	1	23.28	31.28	22.79	30.35	25.66	31.98
	0.9	24.55	31.42	24.41	30.63	26.20	31.34
	0.8	25.10	30.86	25.30	29.74	27.03	28.85
	0.7	7-level	31.96	7-level	31.44	7-level	28.81
	0.6		31.09		30.30		27.69
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
Stepped wave reference	1	19.26	25.63	18.34	25.36	16.85	23.32
	0.9	21.63	25.84	21.37	25	23.13	23.04
	0.8	24.16	26.78	24.37	26.70	26.20	24.18
	0.7	7-level	26.09	7-level	25.78	7-level	22.81
	0.6		25.23		24.88		23.03
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						

Table 5. Vrms for Nine Level Output Voltage based on Equal Amplitude and Unequal Amplitude Carriers with Various Modulation Indices

Ref.	m_a	% THD for 9-level inverter					
		COPWM-A		COPWM-B		COPWM-C	
		EA	UEA	EA	UEA	EA	UEA
Sine reference	1	149	163.7	148.3	164	149.3	162.6
	0.9	139.4	158.3	138.9	157.7	138.7	157.2
	0.8	127.8	152.9	128.2	152.2	124.8	152.5
	0.7	7-level	147.1	7-level	147.1	7-level	146.7
	0.6		139.4		138.7		138.9
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
THI reference	1	168	173.3	168.3	173.9	168.5	174.6
	0.9	157.7	168	156.9	167.6	156.9	168.2
	0.8	146.4	161.9	146.4	161.6	145.3	161.7
	0.7	7-level	154.7	7-level	154.6	7-level	153.7
	0.6		149.7		149.8		148.2
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
Trapezoidal reference	1	166.5	173.3	166.3	173.1	165	173.5
	0.9	157.2	167.5	157.2	167.5	154.6	167.5
	0.8	147.6	162.5	148	162.6	146.4	161.7
	0.7	7-level	154.5	7-level	154.6	7-level	153
	0.6		149.1		148.4		147.9
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
Stepped wave reference	1	149.7	163	148.3	161.9	150.1	161.4
	0.9	139.5	158.5	139.6	157.6	135.7	157.8
	0.8	128.3	151.9	128.7	152.1	122.6	152.1
	0.7	7-level	146.5	7-level	147.4	7-level	146
	0.6		139.7		139.7		140.1
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						

Table 6. Vpeak for Nine Level Output Voltage based on Equal Amplitude and Unequal Amplitude Carriers with Various Modulation Indices

Ref.	m_a	% THD for 9-level inverter					
		COPWM-A		COPWM-B		COPWM-C	
		EA	UEA	EA	UEA	EA	UEA
Sine reference	1	210.8	231.5	209.8	231.9	211.1	229.9
	0.9	197.1	223.9	196.4	223	196.1	222.3
	0.8	180.7	216.2	181.3	215.2	176.5	215.7
	0.7	7-level	208.1	7-level	208	7-level	207.5
	0.6		197.2		196.1		196.5
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
THI reference	1	237.6	245.1	238	245.9	238.3	246.9
	0.9	223	237.6	221.9	237	221.9	237.9
	0.8	207.1	229	207	228.5	205.5	228.6
	0.7	7-level	218.7	7-level	218.6	7-level	217.4
	0.6		211.7		211.8		209.6
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
Trapezoidal reference	1	235.4	245.1	235.2	244.8	233.4	245.3
	0.9	222.3	236.9	222.3	236.9	218.6	236.8
	0.8	208.7	229.7	209.3	230	207.1	228.7
	0.7	7-level	218.5	7-level	218.6	7-level	216.4
	0.6		210.8		209.9		209.2
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
Stepped wave reference	1	211.6	230.6	209.8	228.9	212.2	228.3
	0.9	197.3	224.2	197.4	222.9	191.8	223.2
	0.8	181.5	214.9	182.1	215.1	173.4	215
	0.7	7-level	207.1	7-level	208.5	7-level	206.5
	0.6		197.5		197.6		198.2
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						

Table 7. DC Components for Nine Level Output Voltage based on Equal Amplitude and Unequal Amplitude Carriers with Various Modulation Indices

Ref.	m_a	% THD for 9-level inverter					
		COPWM-A		COPWM-B		COPWM-C	
		EA	UEA	EA	UEA	EA	UEA
Sine reference	1	0.36	0.16	0.00	0.16	0.06	0.11
	0.9	0.38	0.28	0.00	0.17	0.00	0.11
	0.8	0.42	0.40	0.0	0.17	0.00	0.00
	0.7	7-level	0.06	7-level	0.06	7-level	0.06
	0.6		0.19		0.19		0.00
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
THI reference	1	0.11	0.15	0.00	0.15	0.00	0.00
	0.9	0.34	0.16	0.00	0.16	0.00	0.00
	0.8	0.06	0.16	0.00	0.16	0.00	0.00
	0.7	7-level	0.29	7-level	0.17	7-level	0.00
	0.6		0.06		0.18		0.00
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
Trapezoidal reference	1	0.11	0.15	0.00	0.46	0.00	0.20
	0.9	0.00	0.05	0.00	0.16	0.00	0.00
	0.8	0.24	0.16	0.00	0.16	0.00	0.00
	0.7	7-level	0.06	7-level	0.17	7-level	0.00
	0.6		0.30		0.18		0.12
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						
Stepped wave reference	1	0.30	0.81	0.24	0.11	0.47	0.00
	0.9	0.25	0.95	0.00	0.11	0.00	0.00
	0.8	1.45	0.29	0.69	0.12	1.01	0.00
	0.7	7-level	0.24	7-level	0.12	7-level	0.06
	0.6		0.00		0.13		0.00
	0.5						
	0.4	5-level	7-level	5-level	7-level	5-level	7-level
	0.3						

6. CONCLUSION

Various bipolar PWM strategies with equal amplitude carriers and unequal amplitude carriers have been developed using MATLAB-SIMULINK and tested for different modulation indices ranging from 0.8-1 for equal amplitude carriers and 0.6-1 for unequal amplitude carriers for the chosen single phase cascaded ternary multilevel inverter. It is observed from Table 4 that all PWM method provides output with relative low distortion for equal amplitude carriers. If equal voltage sources are chosen then the THD will be less in the case of unequal amplitude carriers. But for the unequal voltage sources the THD is more in the case of unequal amplitude carriers. It is observed from simulation results that (Table-5) almost in all the strategies unequal amplitude carriers gives more fundamental RMS values compared to equal amplitude carriers. It is seen from table 6 that peak voltage is more in the case of unequal amplitude carriers compared to equal amplitude carriers. It is observed from the table 7 that dc components are less in both equal and unequal amplitude carriers.

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