International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 7, No. 3, September 2016, pp. 926~935
ISSN: 2088-8694, DOI: 10.11591/ijpeds. v7.i3.pp926-935

A Novel Control Strategy of Indirect Matrix Converter Using Space Vector Modulation

Kuldeep Behera, Subrat Behera
School of Electrical Enggineering, KIIT University, Bhubaneswar, India

Article Info

Article history:

Received Nov 12, 2015
Revised Apr 6, 2016
Accepted May 7, 2016

Keyword:

Direct matrix converter (DMC)
Indirect matrix converter (IMC)
Matrix converter (MC**)**
Modulation (SVPWM)
Pulse width modulation (PWM)
Space vector modulation (SVM)
Space vector pulse width

ABSTRACT

This paper introduces a control scheme of Indirect Matrix Converter which includes space vector modulation to stabilize the frequency variations. The terminal voltage and frequency of any synchronous machine can be controlled easily with this scheme. Further the control strategy is proposed and implemented in Matlab/Simulink Embedded system which gives significant better performance compared to conventional control technique like better Total Harmonic Distortion (THD), more output voltage with same Modulation Index, less switching stress and less switching loss. This method might prove effective for wind energy conversion system using DFIG as the DFIG speed is close to synchronous speed. The complete control strategy is verified using MATLAB/Simulink.

Corresponding Author:

Kuldeep Behera,
School of Electrical Engineering,
Kalinga Institute of Industrial Technology (KIIT) University,
Bhubaneswar, Odisha, India (751024).
Email: kuldeep.behera.90@gmail.com

1. INTRODUCTION

In a few years the matrix converter has bring considerable attention for its featured operation and efficiency. Basically Matrix converter is a combination of semiconductor switches which gives three phase ac output directly from three phase ac input. It is an alternative to the conventional back to back converter generally used in drives. Indirectly it can be described as a force commutated Cyclo converter. This type of converter also called as single stage AC-AC converter because the input and output currents and sinusoidal. There is no energy storage element between converter and inverter side of the topology. Also the capacitor sizing is a difficult and expensive task in normal back to back converter. The switching scheme of the individual devices is in such a way that a high virtual dc link voltage is created. It can be reduced by either changing the modulation strategy of the converter or inductive-resistive load. Direct Matrix Converter and Indirect Matrix Converter are two different topologies of MC. The performance of IMC is similar to DMC considering input current distortion, no. of devices and bidirectional power flow. Only a drawback of this converter is the input to output voltage ratio is 87% for sinusoidal input and output. Several modulation techniques like PWM, SVPWM, and SVM has already been experimentally implemented by many people. However a digital logic called space vector modulation is successfully applied to matrix converter.

2. INDIRECT MATRIX CONVERTER TOPOLOGY

The source from grid feeds the input terminals of converters where as the output terminals are linked to three phase machine like induction motor. The size of capacitive filter on the voltage feed side

and inductive filter on the current feed side are inversely proposal to switching frequency if the MC. The capacitive filter on the voltage- fed side and the inductive filter on the current-fed side represented in the scheme of MC are intrinsically necessary. Their size is inversely proportional to the matrix converter switching frequency. The IMC is assembled by series connected two mutually anti-parallel connected current link converters and a two level-six switch voltage source converter.

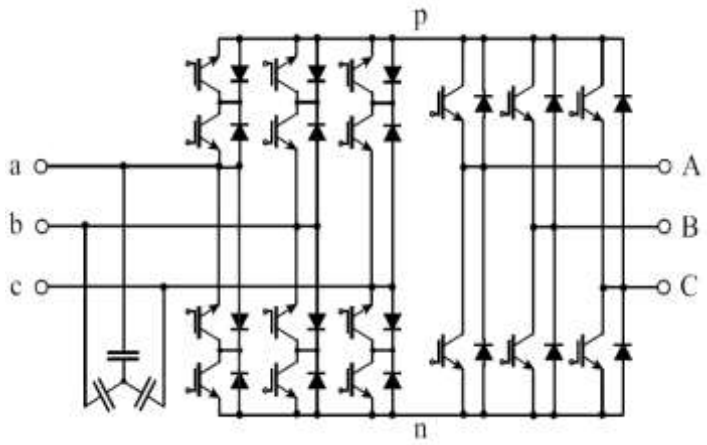

Figure 2.1. Circuit Diagram of Indirect Matrix Converter

Instead of special sensing mechanism of current and voltage, IMC can commutate offering a reduced complexity of choosing modulation. IGBT with reverse blocking has recently available for construction of bi-polar switch having two anti-parallel connected transistors.

2.1. Bidirectional Switch

To implement the four step strategy the bi-directional switches are designed to control the current flow in the circuit. The Figure 2 shows an example of two phase input with a single phase load at output. In steady state both the devices are to be active to allow the current flow. Considering the current flows in load as shown in Figure the upper (S_A) is closed.

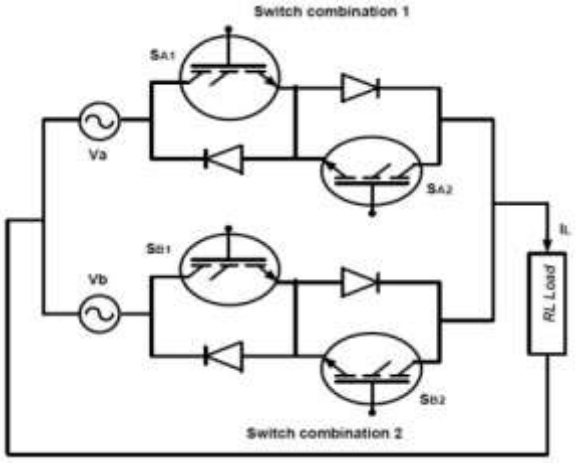

Figure 2.2. Function of 2 level converter

For communication to the lower half (S_B), the device S_{Aa2} is in active state but not conducting. So it is turned off. The reverse in case when S_{Ba} is conducting. The process is shown in the timing diagram. Time delay is dependent on the device characteristics. Advantage of this method is the current conduct in one

switch after another switch with no line-line short circuit and load open circuit. The switching losses is reduced by 50% because of this soft switching process.

2.2. Power Flow in Indirect Matrix Converter

This leg of IMC is considered to be connected to the Input phase "a". This phase "a" is connected to the DC link through the switch S_{pa} and S_{ap} to the positive DC link and S_{na} and S_{an} to the negative DC link. The switches in this topology are arranged in such a manner that bi-directional power flow can take place for both positive and negative DC-Link Voltages. The Figure 2.3(1) and Figure 2.3(2) shows the condition when the DC-Link Voltage is positive and the current direction is positive. In Figure 2.3(1) the current flows from the Rectifier side to the Inverter side through Sap and Dap. In Figure 2.3(2) the current from Inverter side enters Rectifier side phase "a" through D_{na} and S_{na}. The Figure 2.3(3) and Figure 3.3(4) shows the condition when the DC-Link Voltage is negative and the current direction are negative. In Figure 2.3(4) the current flows from the Rectifier side to the Inverter side through D_{an} and S_{an}.

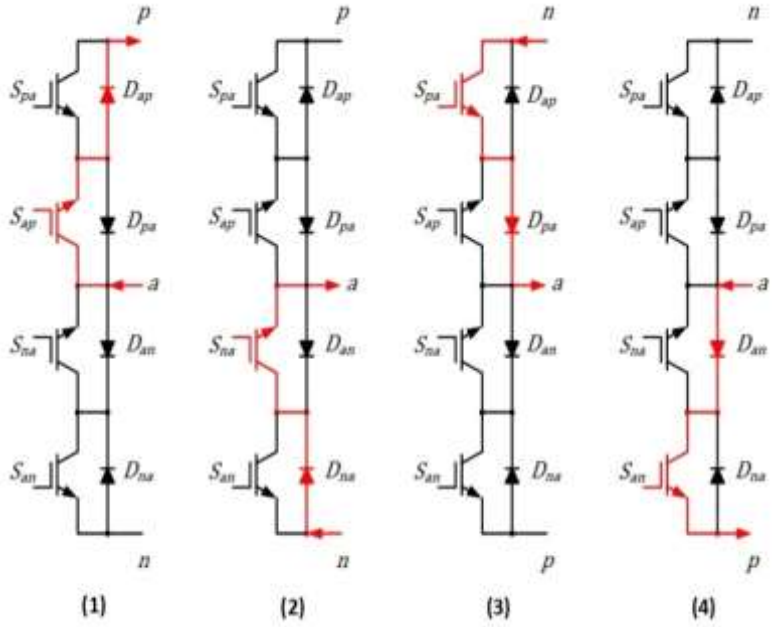

Figure 2.3. Current Flow for Positive Power Flow in One Leg of IMC

In Figure 2.3(3) the current from Inverter side enters Rectifier side phase "a" through S_{pa} and D_{pa}. So, Figure 2.3 explains the bi-directional four quadrant power flow capability of IMC. At this point there is another important concept to note that the inverter stage of the IMC can handle only positive DC-Link polarity.

3. COMMUTATION SCHEME

The inverter input state and rectifier input state have to be performed in order to avoid short circuit and dead time between transistor turn-on or turn-off for a particular switching state. To change from one switching state to another it should to care about that, there should not be any bidirectional path among any input lines having a continuous path for current flow.

3.1. DC-Link Formation

IMC provide freedom in control strategy which reduces the complexity in communication problem.The modulation strategy is devised in such a way that the DC-Link Voltage is always positive. With reference to the symmetry of the circuit topology and an assumed symmetry of the three phases input voltage system the input voltage to the system can be considered as:

$$u_a = \bar{u}_1 \cos(\omega_1 t)$$
$$u_b = \bar{u}_1 \cos(\omega_1 t - 2\pi/3) \quad (3.1.1)$$
$$u_c = \bar{u}_1 \cos(\omega_1 t + 2\pi/3)$$

where, $\bar{u}_1$ is the input peak amplitude and ω_1 is the angular frequency. In order to achieve maximum output voltage, 'a' input phase is clamped to the positive or negative DC link bus for π/3 wide intervals when the corresponding phase voltage has highest value. By implementing this condition, inherently the DC-Link voltage is always kept positive.

For example, at $\phi_1 = \pi/6$

$u_a = 0.875,\ u_b = 0,\ u_c = -0.875$

Hence, $u_{ac} = u_a - u_c = 1.75$

$u_{ab} = u_a - u_b = 0.875$

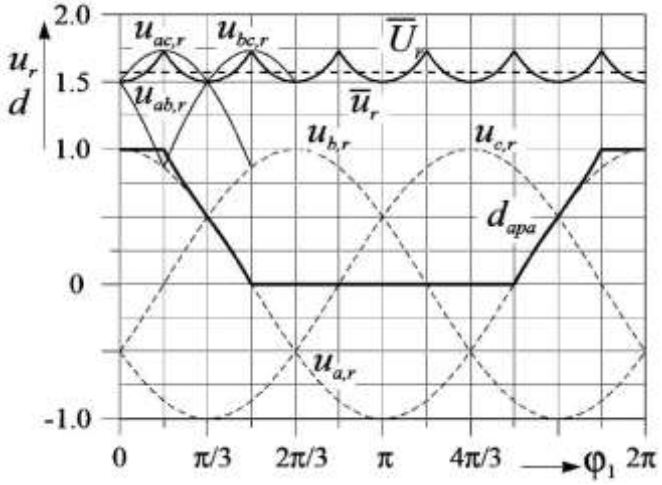

Figure 3.1. Behavior of dc-link voltage and three phase input voltage with average dc-link voltage

Hence this DC-Link voltage u is formed by segments of input line to line voltages. For the period $\phi_1 = 0 \ldots \pi/6$ the DC-Link voltage is formed by the line voltage u_{ac} and u_{ab}. Similarly, for the period $\phi_1 = \pi/6 \ldots . \pi/3$ the DC-Link voltage is formed by the line voltage u_{ac} and u_{bc}. The switching strategy has been designed in such a way that the switching of rectifier occurs at the time of inverter free-wheeling state. In this way the zero DC-link current commutation is achieved. The switching pulses for a pulse period $t_\mu = 0 \ldots \pi/6$ for the rectifier and the inverter stage. In Figure 3.2 the time period T_P has been divided in two equal pulse periods of $T_p/2$. One $T_p/2$ pulse period has been again divided into $T_p/3$and $T_p/6$. To reduce the switching losses the sequence of applied vectors in a half pulse period i.e $t_\mu = 0 \ldots . T_p/2$, is repeated in a reverse direction for the another half pulse period i.e. $t_\mu = T_p/2 \ldots T_p$ as shown.

In the Figure 3.2 S_{Tip} and S_{Tin} (where i denotes either of the input phases "a", "b", "c") denote the switching pulses for the Rectifier switches connected to the positive and negative DC-Link bus respectively. Further, the switching pulse denoted as S_{TI} (where i denotes either of the output phases "A", "B", "C") is applied to the upper switches of the Inverter. In the similar fashion, the switching pulses for other two phase legs of the Rectified section are produced. This switching technique allows the rectifier section of IMC to operate in all the four quadrants of power flow. For the Inverter, the switching pulses for the lower switches are complementary to that of the upper switches. As shown in Figure 4.3 the switching of the Rectifier

switches is done at the free-wheeling states of the Inverter in between the pulse period T_{13}:T_{23} and T_{23}:T_{13}. This reduces complexity in the modulation scheme and to adjust the output voltage zero vector.

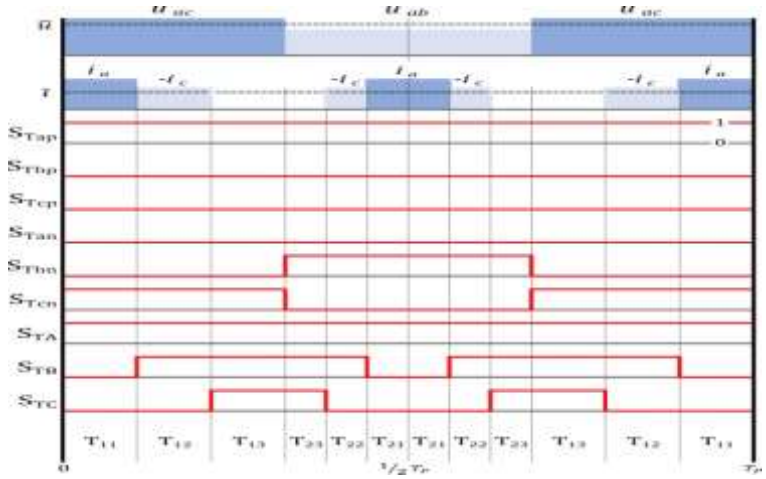

Figure 3.2. Formation of voltage and current for DC-link

3.2. Dwell Time Calculation

For the input to the Rectifier,

$$D_{ac} + D_{ab} = 1 \tag{3.2.1}$$

where, D_{ac} and D_{ab} are the relative on-time of the switches for generation of DC-Link voltage $u=u_{ac}$ and $u=u_{ab}$. For the interval $0...\pi/6$, input phase "a" is clamped to the positive DC-Link bus. The average current of the phases "a", "b", "c" is –

$$i_a = (D_{ab} + D_{ac})i \;,\; i_b = -(D_{ab})i \;,\; i_b = -(D_{ac})i \tag{3.2.2}$$

where, $u_a + u_b + u_c = 0$ has been considered.

The inverter output voltage, u_2 with an absolute value, and a phase value of $\varphi_2 = \omega_2 t = 0 - \pi/6$ is formed over a half pulse period $1/2T_P$ is

$$T_{ac} = \frac{D_{ac}T_p}{2} \;,\; T_{ab} = \frac{D_{ab}T_p}{2} \tag{3.2.3}$$

For generating the reference vector, the location of the reference vector has to be identified. The Space Vectors of MC divide the space vector plane in six sectors and form a hexagon in inverter side as well as rectifier side. The coordination between inverter side hexagon and rectifier side hexagon is done in such way that the zero current switching in the rectifier side can be achieved. To get maximum and symmetrical DC-Link voltage, the each sector of 60^0 duration is divided into two sub-sectors of 30^0 duration. Depending on the reference vector angle on the Space vector hexagon the sub-sector selection has been done.

After the identification of the sub-sector the reference vector is generated by applying the nearby vectors such that the harmonic distortions are less. The nearby vector is applied in such a way that the volt second balance can be achieved. Each nearby vector is applied for certain duration of pulse period. This time periods are known as dwell time period.

The reference vector is generated by applying the nearby vector in a sequence such that at the time of transition from one state to another only one switch on the inverter side as well as rectifier side gets switched. This whole vector sequence is occupied one pulse period. There needs to be introduced a variable which varies from $0...T_P$. On the other hand, the dwell times are divided between vectors according to vector sequence and in a symmetric manner. So, when the variable which is denoted by time 'T' is in between $0...T_{11}$ the vector-1 is applied. Similarly when the variable time the vector-2 is in between T_{11} to $T_{11} + T_{12}$ is supplied.

The vector sequence for generating the reference vector is in such a way that the following condition should be maintained i.e. at the instant of transition from one vector to another vector only one switch gets switched. The switching of more than one switch is not permissible. To reduce the switching losses, the vector sequence for the first half of pulse period is repeated in reverse direction for the second half. The starting vectors should be the ending vector. According to the vector sequence the switching pulse will generate on the other hand according to the value of variable time "T" the vector sequence will be applied in a pulse period.

4. RESULTS AND DISCUSSION

The variation of output voltage with modulation index for same input voltage is verified. Further this theoretical study is validated with simulation study at same specification. The simulation study has been done for the following specifications.

Table 1. Simulation specifications

Sl. No.	Specifications	Rating
1	Maximum input voltage *(U_1)*	120 v
2	Fundamental Frequency *(f)*	50 Hz
3	Rectifier Switching frequency *(f_{swr})*	10 KHz
4	Inverter Switching Frequency *(f_{swi})*	20 KHz
5	3-Φ balanced Load	

The average DC-Link voltage over the pulse period T_P ($\bar{u}$) can be calculated as follows.

$$\bar{u} = \frac{3}{2}\overline{U_1}\frac{1}{\cos(\omega_1 t)} \tag{4.1}$$

where $\omega_1 t$ varies from 0...30 degree in sub sector-1. So, the maximum and the minimum value of the average DC-Link Voltage can be found as given in equation (4.1).

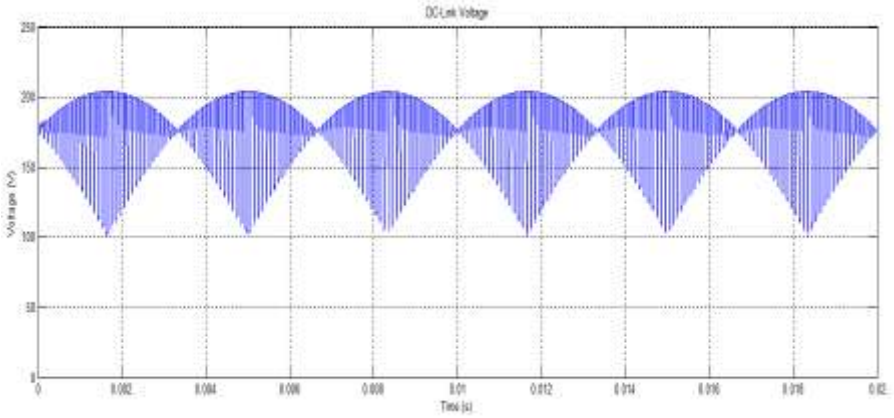

Figure 4.1. DC-Link Voltage of IMC

Assuming modulation index M = 0.8, Peak value of the output phase voltage,

$$\overline{U}_2 = \frac{2}{3}M\overline{U} \tag{4.2}$$

As the inverter part of the IMC is a two level inverter, the phase voltage consists of 5-level and the line voltage consists of 3 level. The voltage level for the phase voltage is $+\frac{2}{3}\overline{U}_{\max}, +\frac{1}{3}\overline{U}_{\max}, 0, -\frac{1}{3}\overline{U}_{\max}, -\frac{2}{3}\overline{U}_{\max}$ similarly for the line voltages the voltage levels are $+\overline{U}_{\max}, 0, -\overline{U}_{\max}$.

Modulation Index 0:8 and above given specification in table the phase voltage levels are 138.56V, 69.28V, 0V, -69.28V, -138.56V and the line voltage levels are 207,84V, 0V, -207.84V.

Considering a star connected balanced load of R=30Ω and L=50mH. This will create an Impedance of Z=33.863Ω. Therefore, RMS-Value of Current is 2.15 A. Voltage stress across a switch is very important aspect that has to take care while designing any power electronic circuit. Depending on the voltage stress the lifespan and the rating of the switching device needs to be decided. The voltage stress across the rectifier switches connected to the positive DC-Link bus (Spi) is shown in as shown in Figure 4.6. The same nature with negative voltage will be obtained in the case of switches connected to the negative DC-Link bus.

In this Figure 4.6, the voltage stress across the switch Si is shown. The voltage across the switch is zero when the switch is "ON" and when the switch is "OFF" negative DC-Link voltage appears across the switch. For positive power flow, in the first sector 0....30 degree the switch Sa is clamped to the positive DC-Link bus hence the voltage across the switch Sa is zero. In the second sector 30....60 degree, S_a operates for a limited time and when the switch is off then the negative DC voltage appears across the switch. Figure 4.8 shows the FFT analysis of output load current with the same R-L load.

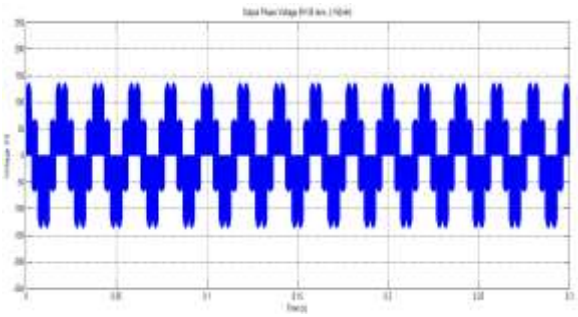

Figure 4.2. Output Phase Voltage of IMC

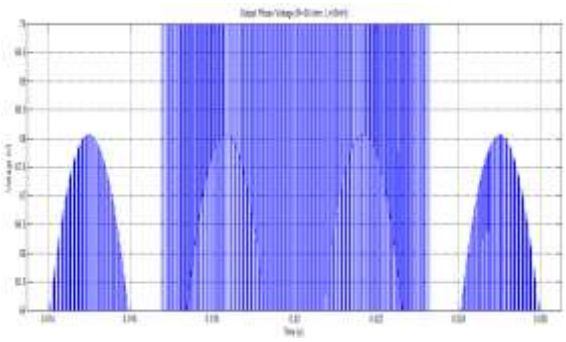

Figure 4.3.(a) Magnified positive side second level Peak Value of Output Phase Voltage

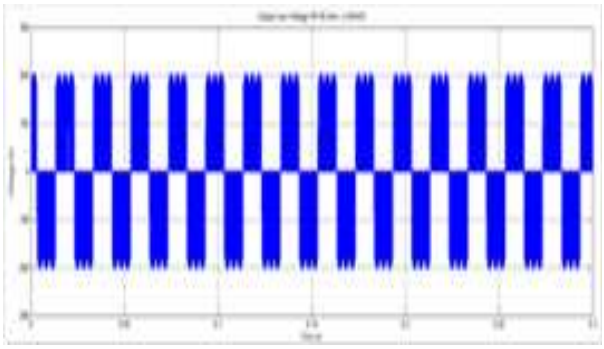

Figure 4.3.(b) Output Line Voltage of IMC

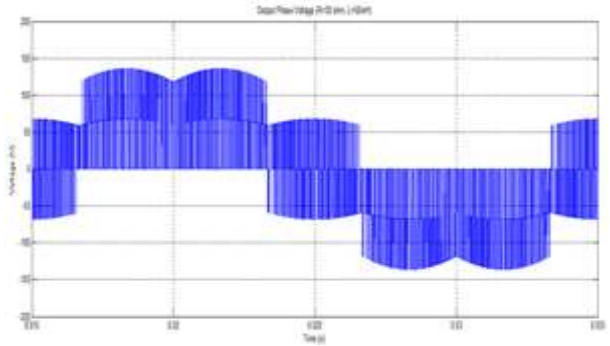

Figure 4.4. One cycle of Output Phase Voltage of IMC

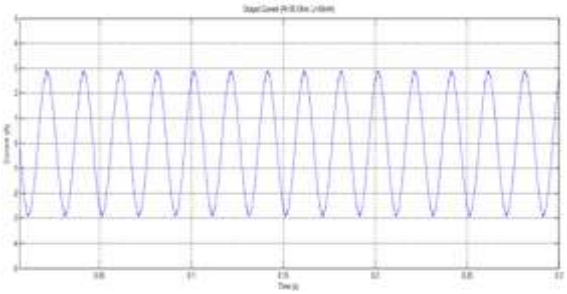

Figure 4.5. Output Phase Current of SMC

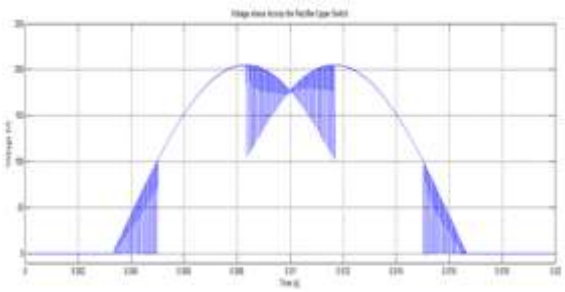

Figure 4.6. Voltage across rectifier upper switch in IMC

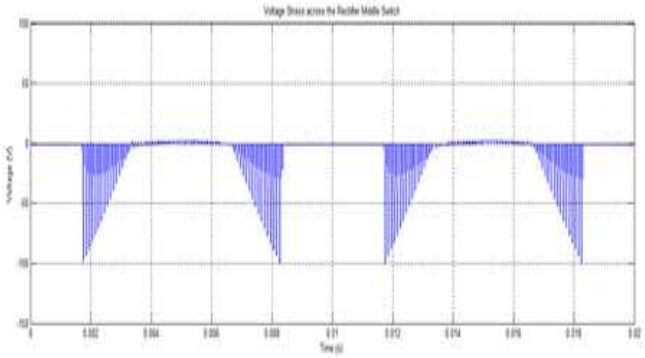

Figure 4.6. Voltage across Rectifier Middle Switch in IMC

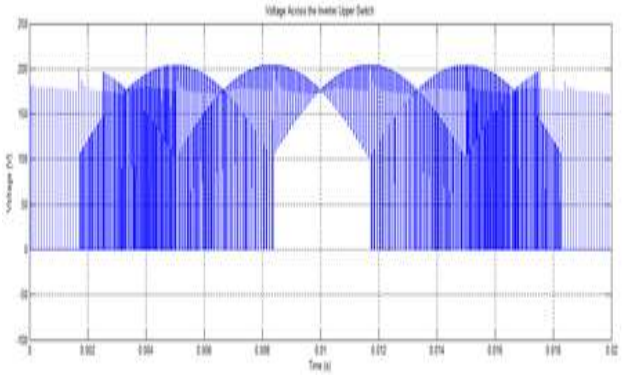

Figure 4.7. Voltage across Inverter Upper Switch in IMC

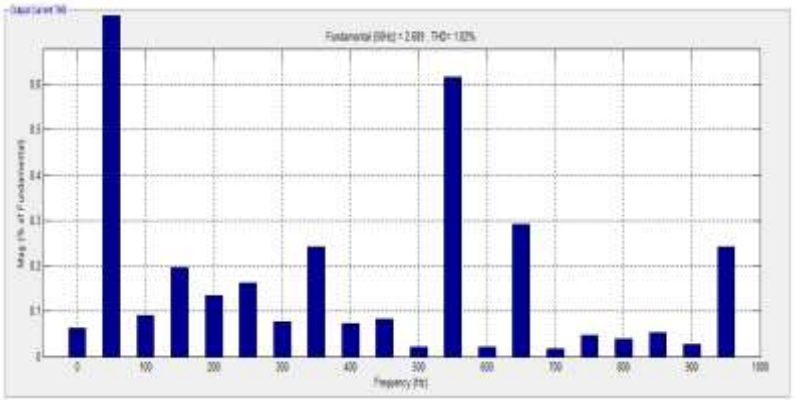

Figure 4.8. THD of Output Current with a load of R = 30 and L = 50 mH

5. CONCLUSION

A detailed analysis has been done of the results. Further the simulation results were also verified with that of the theoretical results. The advantages of Indirect Matrix Converter compared to that of VBBC are shown. It is observed that Indirect Matrix Converters are capable of providing sinusoidal input and output current without the DC-Link capacitor. This is a major advantage regarding reduction in size and cost of AC-AC converter topologies. A significant better performance like better THD, more output voltage with same modulation Index, less switching stress and less switching loss is achieved compared to conventional converter technique.

ACKNOWLEDGEMENT

We would like to thank all faulty members of School of Electrical Engineering, KIIT University for all their technical advice. Also gladly thanks to all staff members of the department for helping in implementing the experimental rig used during research.

REFERENCES

[1] N. Lavanya, M. Venu Gopala Rao, Control of Indirect Matrix Converter by Using Improved SVM Method, *International Journal of Power Electronics and Drive System*, Vol. 6, No. 2, June 2015, pp. 370~375.
[2] Mutharasan A, Rameshkumar T, Ajitha A,Wind Energy Conversion Based On Matrix Converter, *International Journal of Power Electronics and Drive System*, Vol. 5, No. 1, July 2014, pp. 119~128.
[3] Ruben Pena, Roberto Cardenas, Eduardo Reyes, Jon Clare and Patrick Wheeler, Control of a Doubly Fed Induction Generator via an Indirect Matrix Converter With Changing DC Voltage, *IEEE Transactions On Industrial Electronics*, Vol. 58, No. 10, October 2011.
[4] J. Karpagam, Dr. A. Nirmal Kumar and V. Kumar Chinnaiyan, Comparison of Modulation Techniques for Matrix Converter, *IACSIT International Journal of Engineering and Technology*, Vol. 2, No. 2, April 2010.
[5] Johann W. Kolar, Simon D. Round, Novel Three-Phase AC–AC Sparse Matrix Converters, *IEEE Transactions On Power Electronics*, Vol. 22, No. 5, September 2007.
[6] Mahmoud Hamouda, Farhat Fnaiech and Kamal Al-Haddad, *Space Vector Modulation Scheme for Dual-Matrix Converters using Safe-Commutation Strategy*, IECON 2005, IEEE 31st Annual Conference on Industrial Electronics, pp.1060-1065, Nov 2005.
[7] L. Helle, K.B. Larsen, A.H. Jorgensen, S. Munk-Nielsen, and F. Blaabjerg, Evaluation of Modulation Schemes for Three-phase to Three-phase Matrix Converters, *IEEE Trans. Ind. Electron*., vol. 51, Feb. 2004.
[8] Apap, M. Clare, J.C. Wheeler and P.W. Bradley, K.J. , *Analysis and Comparison of AC-AC Matrix Converter Control Strategies, PESC03*, IEEE 34th Annual conference on Power Electronics, Vol. 3, pp. 1287-1292, June 2003.
[9] P. Wheeler, J. Rodriguez, J. Clare, L. Empringham, and A. Weinstein, Matrix converters: A technology review, *IEEE Trans. Ind. Electron*., vol. 49, Apr 2002.
[10] P. Zwimpfer and H. Stemmler, *Modulation and Realization of a Novel Two-stage Matrix Converter*, in Proc. Brazilian Power Electronics Conf., Florianópolis, Brazil, Nov. 11–14, 2001.

BIOGRAPHIES OF AUTHORS

Kuldeep Behera received the Bachelors degree from the Biju Patnaik University of Technology, Odisha, India in Applied Electronics & Instrumentation in year 2012, Master degree from KIIT University, India in Electrical Engineering with specialization Power and Energy System in 2016. Also he has industrial experience of in automation sector. Currently he is a P.G. scholar as well as teaching assistant in KIIT university. His main research interests include electricity generation from renewable-energy systems.

Subrat Behera received the Bachelors degree from National Institute of Technolgy, Nagpur, India in year 2007 in Electrical Engineering and Post graduation from Indian Institute of Technology, Roorkee, India in year 2009 with specialization Electric Drives & Power system. Now he is assistant professor in KIIT university in Electrical engineering department since 2009. His main research interests include application of power electronics in renewable energy sources.