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Modeling and Simulation of 127 Level Optimal Multilevel Inverter with Lower Number of Switches and Minimum THD

Bolla Madhusudana Reddy[1], Y. V. Siva Reddy[2], M. Vijaya Kumar[3]
[1]Electrical Engineering, JNTUA, Anathapuaramu, Andhraparadesh, India
[2]Department of Electrical & Electronics Engineering, G.Pulla Reddy Engineering College, Andhraparadesh, India
[3] Department of Electrical & Electronics Engineering, JNTUA College of Engineering, Anatapur, Andhraparadesh, India

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ABSTRACT

This paper proposes a new optimal high level multilevel inverter with minimum number of components. This multi level inverter (MLI) is designed with series combination of basic units which can generate positive levels at output. DC source values applied for each basic unit is different with another. An H bridge is connected across proposed MLI for generating negative levels along with positive levels at output and that inverter considered as proposed high level optimal multilevel inverter. Single unit is responsible producing 21 levels. Therefore six units are connected in cascaded form to increase number of levels as 127 at output. Decrease in the number of power switches, driver circuits, and dc voltage sources are the improvement of the proposed MLI. Sinusoidal multiple pulse width modulation (SPWM) technique is implemented to produce pulses for turning ON switches according requirement. Low total harmonic distortion at output voltage or current production is major advantage of proposed module. The validations of proposed MLI results are verified through MATLAB/SIMULINK.

Corresponding Author:

B. Madhusudana Reddy,
Electrical Engineering
JNTUA College of Engineering,
Anatapur, Andhraparadesh, India.
Email: madhusudhanareddy.bolla@gmail.com

1. INTRODUCTION

The power semi conductor switches cannot able to connect directly to high voltage network. The high-voltage high power with stand inverters demand is increasing day by day, in order to meet high voltage high power demand multilevel inverters are have been developed. By increasing number of levels at output wave form two main advantages are obtained one is sinusoidal like wave form at output and another is reduced total harmonic distortion in the output voltage and current waveform. In addition to that, minimum switching losses, voltage stress on switches are less[1-5].Mainly three types of traditional multilevel inverters are exist such as (i) neutral point clamped MLIs, (ii) flying-capacitor MLIs, (iii) cascaded H bridge type MLIs [6–9]. Cascaded multilevel inverters did not use diode clamped and/or flying capacitors for achieving reliability, modularity, simple control and lower number of switches [10-11]. Hence the switching losses and overall cost of proposed inverters decreases and efficiency can be improved [12].Various types of symmetric and asymmetric cascaded multilevel inverters presented in [13]–[18]. Two algorithms are presented like symmetric and asymmetric presented in [19]. Different asymmetric cascaded multilevel inverters have been presented for increasing the number of output levels in [20].

Basically six switch inverters were frequently used in industrial applications, but this type of inverters are not appropriate for low power applications due to very high switching losses and complexity

exist control method. The major problems facing of conventional type MLIs are more number of switching devices, switching losses, standing voltages and high THD.

Cascaded multilevel inverters are designed with series of basic units. Each basic unit consists of dc sources and switches. These are categorized in two ways one is symmetrical type where all dc sources are equal in all basic units, and other is asymmetrical type where dc sources are different in each basic unit. The asymmetric cascaded multilevel inverters produce a more levels in output with minimum switches while compared with symmetric cascaded multilevel inverters due to the cause of the various magnitudes of dc voltage sources. Hence space and cost of an asymmetric cascaded multilevel inverter is less than that of a symmetric cascaded multilevel inverter.The proposed novel series connected high level assymetricl type optimal MLI produces less THD when compare to classical type same high level assymetrical MLI.

2. RESEARCH METHOD

The classical 127 level multilevel inverter is series combination of six H-bridge inverters is as shown in Figure 1. Each H -Bridge contains four switches and one dc source. The magnitudes dc sources are applied in the ratio of 1:2:4:8:16:32 for individual H bridges to achieve 127 level at output. The positive levels at output obtained by turning ON the S_{n2} & S_{n3} switches, where as for negative levels are obtained with turning On of S_{n1} &S_{n4} switches. All the switches are unidirectional IGBTs Load should be connected across series string of H bridges.

$$N_{switch}=4n;\ n \geq 1 \quad (1)$$

$$N_{drivers}=4n \quad (2)$$

$$N_{source}=n \quad (3)$$

$$N_{level}=2^{(n+1)}-1 \quad (4)$$

'n' indicates number of cascaded basic H bridge units,$N_{switch,}$ means number of switches, $N_{drivers}$ indicates gate drivers, N_{source} means number of dc sources and N_{level} number of levels generated at output.

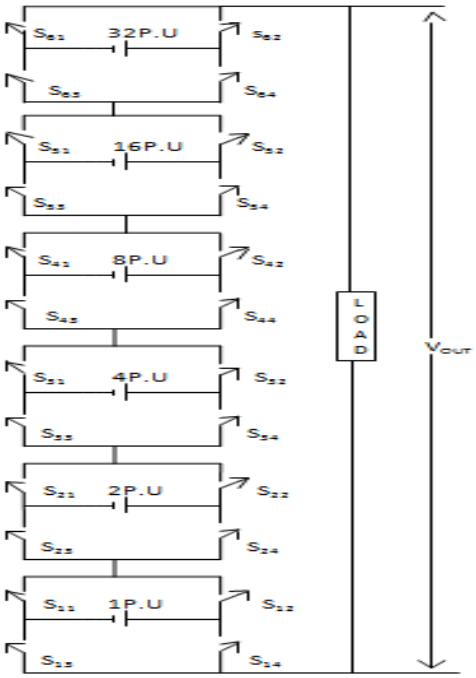

Figure 1.Classical 127 level H-Bridge multilevel inverter

Table 1 shows the ON state representation of switches and with their magnitudes of dc sources of respective H Bridge units. Suppose to get positive 63 level output, all H bridge sources added by turning ON the S_{m2}&S_{m3} switches, where similarly to obtain negative 63 level output, all H bridge sources added with turning ON the S_{m1} & S_{m4} switches. Where m=1, 2, 3, 4, 5, 6 …..n. If suppose any one of particular bridge dc source not added to get desired output level that source is by passed through upper and lower switches same limb of related H bridge. For example to get positive 62 level at output 1 PU dc source is not required by turning ON the S_{11} & S_{13} switches and for negative 62 level output case S_{12} &S_{14} should be turn ON for by passing 1 PU dc source.

Table 1. ON State Switching Pattern Sources for Classical 127 Level Multilevel Inverter

Voltage (per unit)	Switching patterns with sources	Voltage (per unit)	Switching patterns with sources	Voltage (per unit)	Switching patterns with sources
63	1+2+4+8+16+32	62	2+4+8+16+32	61	1+4+8+16+32
60	4+8+16+32	59	1+2+8+16+32	58	2+8+16+32
57	1+8+16+32	56	8+16+32	55	1+2+4+16+32
54	2+4+16+32	53	1+4+16+32	52	4+16+32
51	1+2+16+32	50	2+16+32	49	1+16+32
48	16+32	47	1+2+4+8+32	46	2+4+8+32
45	1+4+8+32	44	4+8+32	43	1+2+8+32
42	2+8+32	41	1+8+32	40	8+32
39	1+2+4+32	38	2+4+32	37	1+4+32
36	4+32	35	1+2+32	34	2+32
33	1+32	32	32	31	1+2+4+8+16
30	2+4+8+16	29	1+4+8+16	28	4+8+16
27	1+2+8+16	26	2+8+16	25	1+8+16
24	8+16	23	1+2+4+16	22	2+4+16
21	1+4+16	20	4+16	19	1+2+16
18	2+16	17	1+16	16	16
15	1+2+4+8	14	2+4+8	13	1+4+8
12	4+8	11	1+2+8	10	2+8
9	1+8	8	8	7	1+2+4
6	2+4	5	1+4	4	4
3	1+2	2	2	1	1
0	0	-1	-1	-2	-2
-3	-1-2	-4	-4	-5	-1-4
-6	-2-4	-7	-1-2-4	-8	-8
-9	-1-8	-10	-2-8	-11	-1-2-8
-12	-4-8	-13	-1-4-8	-14	-2-4-8
-15	-1-2-4-8	-16	-16	-17	-1-16
-18	-2-16	-19	-1-2-16	-20	-4-16
-21	-1-4-16	-22	-2-4-16	-23	-1-2-4-16
-24	-8-16	-25	-1-8-16	-26	-2-8-16
-27	-1-2-8-16	-28	-4-8-16	-29	-1-4-8-16
-30	-2-4-8-16	-31	-1-2-4-8-16	-32	-32
-33	-1-32	-34	-2-32	-35	-1-2-32
-36	-4-32	-37	-1-4-32	-38	-2-4-32
-39	-1-2-4-32	-40	-8-32	-41	-1-8-32
-42	-2-8-32	-43	-1-2-8-32	-44	-4-8-32
-45	-1-4-8-32	-46	-2-4-8-32	-47	-1-2-4-8-32
-48	-16-32	-49	-1-16-32	-50	-2-16-32
-51	-1-2-16-32	-52	-4-16-32	-53	-1-4-16-32
-54	-2-4-16-32	-55	-1-2-4-8-16-32	-56	-8-16-32
-57	-1-8-16-32	-58	-2-8-16-32	-59	-1-2-8-16-32
-60	-4-8-16-32	-61	-1-4-8-16-32	-62	-2-4-8-16-32
-63	-1-2-4-8-16-32				

Figure 2 shows the proposed 127 level optimal multilevel inverter made with cascaded connection of six basic units. Each basic unit consists of on dc source and two switches. In ratio of 1:2:4:8:16:32.In general the dc source magnitudes expressed as shown Equation 5

$$V_{dc,i}=(2)^{(i-1)}*V_{dc,1} \quad (5)$$

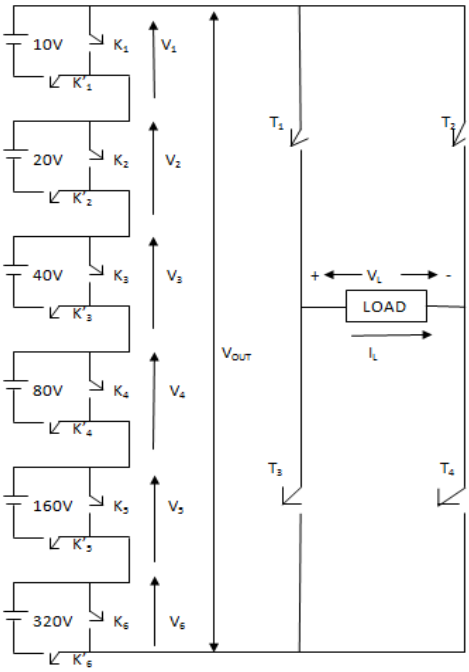

Figure 2. Proposed 127 level optimal multilevel inverter

$V_{dc,1}$ is minimum or first basic unit input dc voltage , and i=1, 2, 3….n; where 'n' means number of cascaded connected basic units .In this proposed module $V_{dc,1}$=10V.

$$N_{SWITCH}=2n + 4, \text{ for } n \geq 1 \quad (6)$$

$$N_{DRIVER}=N_{SWITCH} \quad (7)$$

$$N_{IGBT=}2n + 4 \quad (8)$$

$$N_{SOURCE}=n \quad (9)$$

$$\text{Output level number } N_{LEVEL=}2^{n+1} - 1 \quad (10)$$

Where, $N_{SWITCH,}$, $N_{DRIVER,}$, N_{IGBT} , and $N_{SOURCE,}$ are the number of switches, number of switches' drivers, number of IGBTs, and number of sources respectively.

Table 2 shows ON states of switches for proposed 127 level optimal multilevel inverter. Suppose in order to get output as +63 level ,all series connected switches S'_i required to be turn ON ,where i=1,2,3,4,5,6…n., addition to T_1 and T_4 switches should be ON. Similarly to get -63 level output, all series connected switches S_i required to turned ON where i=1, 2, 3, 4, 5, 6…n in addition to T_2 and T_3 should be ON. Thus to achieve positive level output T_1&T_4 ON in H bridge, and for negative level output purpose T_2 and T_3 should be ON. Finally say that series switches will enhances the level number but shunt switches decrease the level number.AS the number of levels at output side increases the wave form would be more sinusoidal so that total harmonic distortion decreases.

Table 2. ON State Switching Pattern for Proposed 127 Level Optimal MLI

Voltage (P.U)	ON Switching patterns	Level No.	Voltage (P.U)	ON Switching patterns	Level No.
+63	$K'_1+K'_2+K'_3+K'_4+K'_5+K'_6+T_1+T_4$	127	+62	$K_1+K'_2+K'_3+K'_4+K'_5+K'_6+T_1+T_4$	126
+61	$K'_1+K_2+K'_3+K'_4+K'_5+K'_6+T_1+T_4$	125	+60	$K_1+K_2+K'_3+K'_4+K'_5+K'_6+T_1+T_4$	124
+59	$K'_1+K'_2+K_3+K'_4+K'_5+K'_6+T_1+T_4$	123	+58	$K_1+K'_2+K_3+K'_4+K'_5+K'_6+T_1+T_4$	122
+57	$K'_1+K_2+K_3+K'_4+K'_5+K'_6+T_1+T_4$	121	+56	$K_1+K_2+K_3+K'_4+K'_5+K'_6+T_1+T_4$	120
+55	$K'_1+K'_2+K'_3+K_4+K'_5+K'_6+T_1+T_4$	119	+54	$K_1+K'_2+K'_3+K_4+K'_5+K'_6+T_1+T_4$	118
+53	$K'_1+K_2+K'_3+K_4+K'_5+K'_6+T_1+T_4$	117	+52	$K_1+K_2+K'_3+K_4+K'_5+K'_6+T_1+T_4$	116
+51	$K'_1+K'_2+K_3+K_4+K'_5+K'_6+T_1+T_4$	115	+50	$K_1+K'_2+K_3+K_4+K'_5+K'_6+T_1+T_4$	114
+49	$K'_1+K_2+K_3+K_4+K'_5+K'_6+T_1+T_4$	113	+48	$K_1+K_2+K_3+K_4+K'_5+K'_6+T_1+T_4$	112
+47	$K'_1+K'_2+K'_3+K'_4+K_5+K'_6+T_1+T_4$	111	+46	$K_1+K'_2+K'_3+K'_4+K_5+K'_6+T_1+T_4$	110
+45	$K'_1+K_2+K'_3+K'_4+K_5+K'_6+T_1+T_4$	109	+44	$K_1+K_2+K'_3+K'_4+K_5+K'_6+T_1+T_4$	108
+43	$K'_1+K'_2+K'_3+K_4+K_5+K'_6+T_1+T_4$	107	+42	$K_1+K'_2+K_3+K'_4+K_5+K'_6+T_1+T_4$	106
+41	$K'_1+K_2+K_3+K'_4+K_5+K'_6+T_1+T_4$	105	+40	$K_1+K_2+K_3+K'_4+K_5+K'_6+T_1+T_4$	104
+39	$K'_1+K'_2+K'_3+K_4+K_5+K'_6+T_1+T_4$	103	+38	$K_1+K'_2+K'_3+K_4+K_5+K'_6+T_1+T_4$	102
+37	$K'_1+K_2+K'_3+K_4+K_5+K'_6+T_1+T_4$	101	+36	$K_1+K_2+K'_3+K_4+K_5+K'_6+T_1+T_4$	100
+35	$K'_1+K'_2+K_3+K_4+K_5+K'_6+T_1+T_4$	99	+34	$K_1+K'_2+K_3+K_4+K_5+K'_6+T_1+T_4$	98
+33	$K'_1+K_2+K_3+K_4+K_5+K'_6+T_1+T_4$	97	+32	$K_1+K_2+K_3+K_4+K_5+K'_6+T_1+T_4$	96
+31	$K'_1+K'_2+K'_3+K'_4+K'_5+K_6+T_1+T_4$	95	+30	$K_1+K'_2+K'_3+K'_4+K'_5+K_6+T_1+T_4$	94
+29	$K'_1+K_2+K'_3+K'_4+K'_5+K_6+T_1+T_4$	93	+28	$K_1+K_2+K'_3+K'_4+K'_5+K_6+T_1+T_4$	92
+27	$K'_1+K'_2+K_3+K'_4+K'_5+K_6+T_1+T_4$	91	+26	$K_1+K'_2+K_3+K'_4+K'_5+K_6+T_1+T_4$	90
+25	$K'_1+K_2+K_3+K'_4+K'_5+K_6+T_1+T_4$	89	+24	$K_1+K_2+K_3+K'_4+K'_5+K_6+T_1+T_4$	88
+23	$K'_1+K'_2+K'_3+K_4+K'_5+K_6+T_1+T_4$	87	+22	$K_1+K'_2+K'_3+K_4+K'_5+K_6+T_1+T_4$	86
+21	$K'_1+K_2+K'_3+K_4+K'_5+K_6+T_1+T_4$	85	+20	$K_1+K_2+K'_3+K_4+K'_5+K_6+T_1+T_4$	84
+19	$K'_1+K'_2+K_3+K_4+K'_5+K_6+T_1+T_4$	83	+18	$K_1+K'_2+K_3+K_4+K'_5+K_6+T_1+T_4$	82
+17	$K'_1+K_2+K_3+K_4+K'_5+K_6+T_1+T_4$	81	+16	$K_1+K_2+K_3+K_4+K'_5+K_6+T_1+T_4$	80
+15	$K'_1+K'_2+K'_3+K'_4+K_5+K_6+T_1+T_4$	79	+14	$K_1+K'_2+K'_3+K'_4+K_5+K_6+T_1+T_4$	78
+13	$K'_1+K_2+K'_3+K'_4+K_5+K_6+T_1+T_4$	77	+12	$K_1+K_2+K'_3+K'_4+K_5+K_6+T_1+T_4$	76
+11	$K'_1+K'_2+K_3+K'_4+K_5+K_6+T_1+T_4$	75	+10	$K_1+K'_2+K_3+K'_4+K_5+K_6+T_1+T_4$	74
+9	$K'_1+K_2+K_3+K'_4+K_5+K_6+T_1+T_4$	73	+8	$K_1+K_2+K_3+K'_4+K_5+K_6+T_1+T_4$	72
+7	$K'_1+K'_2+K'_3+K_4+K_5+K_6+T_1+T_4$	71	+6	$K_1+K'_2+K'_3+K_4+K_5+K_6+T_1+T_4$	70
+5	$K'_1+K_2+K'_3+K_4+K_5+K_6+T_1+T_4$	69	+4	$K_1+K_2+K'_3+K_4+K_5+K_6+T_1+T_4$	68
+3	$K'_1+K'_2+K_3+K_4+K_5+K_6+T_1+T_4$	67	+2	$K_1+K'_2+K_3+K_4+K_5+K_6+T_1+T_4$	66
+1	$K'_1+K_2+K_3+K_4+K_5+K_6+T_1+T_4$	65	0	$K_1+K_2+K_3+K_4+K_5+K_6$	64
-1	$K'_1+K_2+K_3+K_4+K_5+K_6+T_2+T_3$	63	-2	$K_1+K'_2+K_3+K_4+K_5+K_6+T_2+T_3$	62
-3	$K'_1+K'_2+K_3+K_4+K_5+K_6+T_2+T_3$	61	-4	$K_1+K_2+K'_3+K_4+K_5+K_6+T_2+T_3$	60
-5	$K'_1+K_2+K'_3+K_4+K_5+K_6+T_2+T_3$	59	-6	$K_1+K'_2+K'_3+K_4+K_5+K_6+T_2+T_3$	58
-7	$K'_1+K'_2+K'_3+K_4+K_5+K_6+T_2+T_3$	57	-8	$K_1+K_2+K_3+K'_4+K_5+K_6+T_2+T_3$	56
-9	$K'_1+K_2+K_3+K'_4+K_5+K_6+T_2+T_3$	55	-10	$K_1+K'_2+K_3+K'_4+K_5+K_6+T_2+T_3$	54
-11	$K'_1+K'_2+K_3+K'_4+K_5+K_6+T_{12}+T_3$	53	-12	$K_1+K_2+K'_3+K'_4+K_5+K_6+T_2+T_3$	52
-13	$K'_1+K_2+K'_3+K'_4+K_5+K_6+T_2+T_3$	51	-14	$K_1+K'_2+K'_3+K'_4+K_5+K_6+T_2+T_3$	50
-15	$K'_1+K'_2+K'_3+K'_4+K_5+K_6+T_2+T_3$	49	-16	$K_1+K_2+K_3+K_4+K'_5+K_6+T_2+T_3$	48
-17	$K'_1+K_2+K_3+K_4+K'_5+K_6+T_2+T_3$	47	-18	$K_1+K'_2+K_3+K_4+K'_5+K_6+T_2+T_3$	46
-19	$K'_1+K'_2+K_3+K_4+K'_5+K_6+T_2+T_3$	45	-20	$K_1+K_2+K'_3+K_4+K'_5+K_6+T_2+T_3$	44
-21	$K'_1+K_2+K'_3+K_4+K'_5+K_6+T_2+T_3$	43	-22	$K_1+K'_2+K'_3+K_4+K'_5+K_6+T_2+T_3$	42
-23	$K'_1+K'_2+K'_3+K_4+K'_5+K_6+T_2+T_3$	41	-24	$K_1+K_2+K_3+K'_4+K'_5+K_6+T_2+T_3$	40
-25	$K'_1+K_2+K_3+K'_4+K'_5+K_6+T_2+T_3$	39	-26	$K_1+K'_2+K_3+K'_4+K'_5+K_6+T_2+T_3$	38
-27	$K'_1+K'_2+K_3+K'_4+K'_5+K_6+T_2+T_3$	37	-28	$K_1+K_2+K'_3+K'_4+K'_5+K_6+T_2+T_3$	36
-29	$K'_1+K_2+K'_3+K'_4+K'_5+K_6+T_2+T_3$	35	-30	$K_1+K'_2+K'_3+K'_4+K'_5+K_6+T_2+T_3$	34
-31	$K'_1+K'_2+K'_3+K'_4+K'_5+K_6+T_2+T_3$	33	-32	$K_1+K_2+K_3+K_4+K_5+K'_6+T_2+T_3$	32
-33	$K'_1+K_2+K_3+K_4+K_5+K'_6+T_2+T_3$	31	-34	$K_1+K'_2+K_3+K_4+K_5+K'_6+T_2+T_3$	30
-35	$K'_1+K'_2+K_3+K_4+K_5+K'_6+T_2+T_3$	29	-36	$K_1+K_2+K'_3+K_4+K_5+K'_6+T_2+T_3$	28
-37	$K'_1+K_2+K'_3+K_4+K_5+K'_6+T_2+T_3$	27	-38	$K_1+K'_2+K'_3+K_4+K_5+K'_6+T_2+T_3$	26
-39	$K'_1+K'_2+K'_3+K_4+K_5+K'_6+T_2+T_3$	25	-40	$K_1+K_2+K_3+K'_4+K_5+K'_6+T_2+T_3$	24
-41	$K'_1+K_2+K_3+K'_4+K_5+K'_6+T_2+T_3$	23	-42	$K_1+K'_2+K_3+K'_4+K_5+K'_6+T_2+T_3$	22
-43	$K'_1+K'_2+K'_3+K_4+K_5+K'_6+T_2+T_3$	21	-44	$K_1+K_2+K'_3+K'_4+K_5+K'_6+T_2+T_3$	20
-45	$K'_1+K_2+K'_3+K'_4+K_5+K'_6+T_2+T_3$	19	-46	$K_1+K'_2+K'_3+K'_4+K_5+K'_6+T_2+T_3$	18
-47	$K'_1+K'_2+K'_3+K'_4+K_5+K'_6+T_2+T_3$	17	-48	$K_1+K_2+K_3+K_4+K'_5+K'_6+T_2+T_3$	16
-49	$K'_1+K_2+K_3+K_4+K'_5+K'_6+T_2+T_3$	15	-50	$K_1+K'_2+K_3+K_4+K'_5+K'_6+T_2+T_3$	14
-51	$K'_1+K'_2+K_3+K_4+K'_5+K'_6+T_2+T_3$	13	-52	$K_1+K_2+K'_3+K_4+K'_5+K'_6+T_2+T_3$	12
-53	$K'_1+K_2+K'_3+K_4+K'_5+K'_6+T_2+T_3$	11	-54	$K_1+K'_2+K'_3+K_4+K'_5+K'_6+T_2+T_3$	10
-55	$K'_1+K'_2+K'_3+K_4+K'_5+K'_6+T_2+T_3$	9	-56	$K_1+K_2+K_3+K'_4+K'_5+K'_6+T_2+T_3$	8
-57	$K'_1+K_2+K_3+K'_4+K'_5+K'_6+T_2+T_3$	7	-58	$K_1+K'_2+K_3+K'_4+K'_5+K'_6+T_2+T_3$	6
-59	$K'_1+K'_2+K_3+K'_4+K'_5+K'_6+T_2+T_3$	5	-60	$K_1+K_2+K'_3+K'_4+K'_5+K'_6+T_2+T_3$	4
-61	$K'_1+K_2+K'_3+K'_4+K'_5+K'_6+T_2+T_3$	3	-62	$K_1+K'_2+K'_3+K'_4+K'_5+K'_6+T_2+T_3$	2
-63	$K'_1+K'_2+K'_3+K'_4+K'_5+K'_6+T_2+T_3$	1			

3. SIMULATION RESULTS AND DISCUSSION

In classical topology 24 number of switches are used but in proposed topology 16 number of switches used only therefore switching losses can be minimized in proposed topology hence output power

and efficiency can be improved. Classical MLI fundamental voltage is 605.4v which is less than proposed MLI topology of 623.1v.Proposed topology produces 127 levels at output as shown in Figure 4 and total harmonic distortion is 0.96% as shown in Figure 5 which is less than of classical 127 level MLI topology of total harmonic distrotion is 1.74% as shown in Figure 6. Thus by increasing number of levels quality sinusoidal waveform achieved with minimum THD. Table 3 shows comparison table between single phase classical and proposed MLIs.

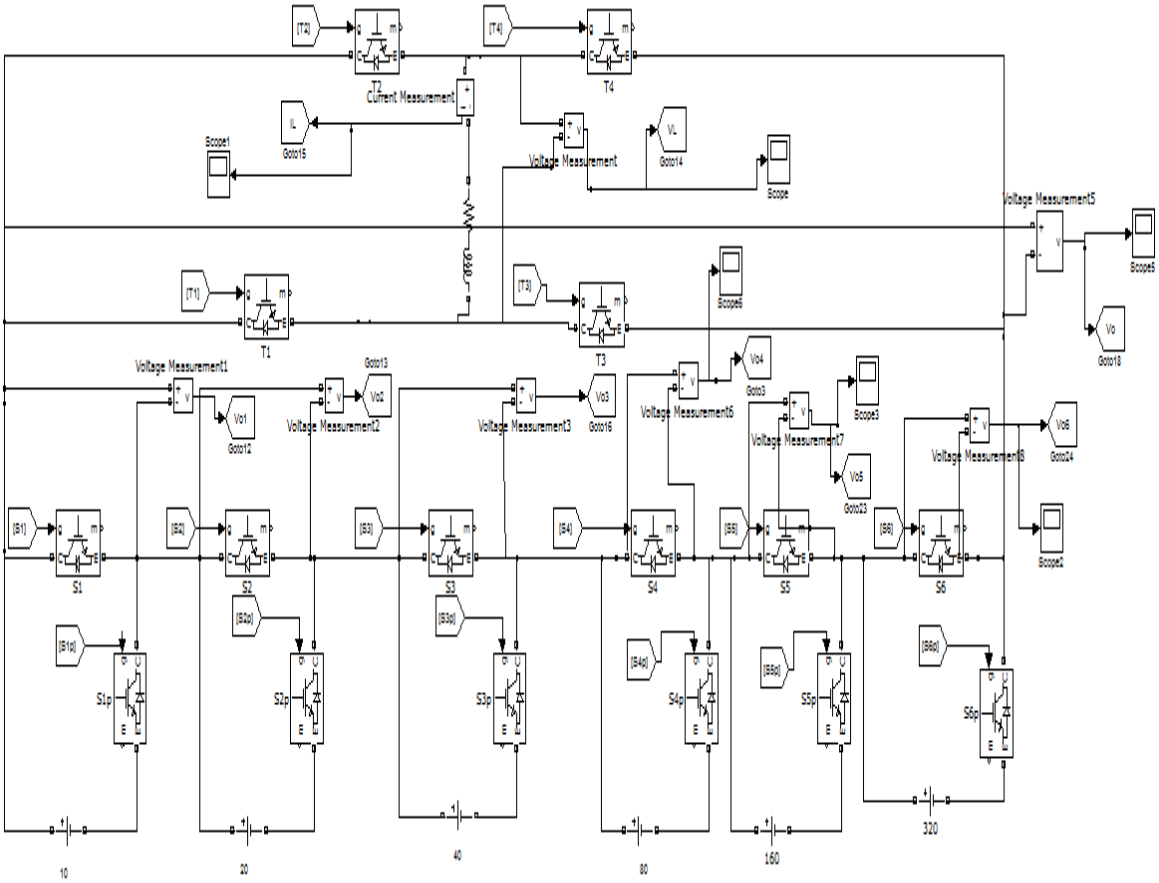

Figure 3. Simulation diagram of single phase proposed127 level optimal multilevel inverter

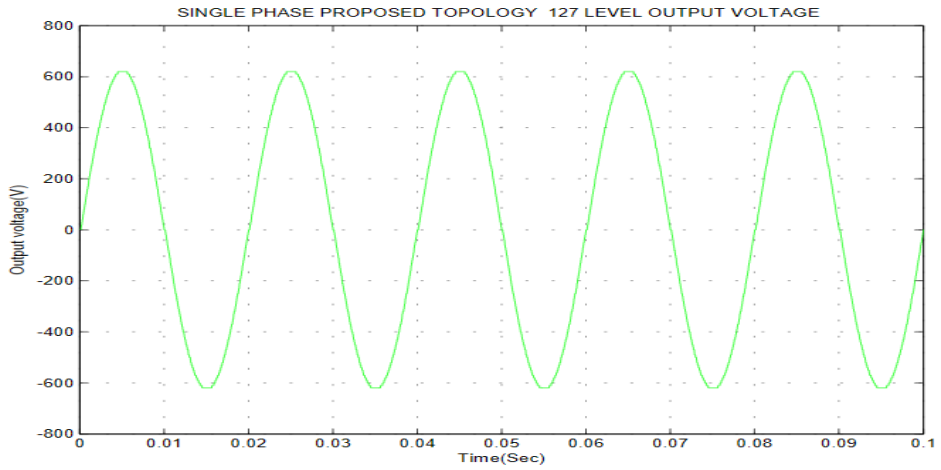

Figure 4. Single phase proposed127 level optimal multilevel inverter output voltage wave form

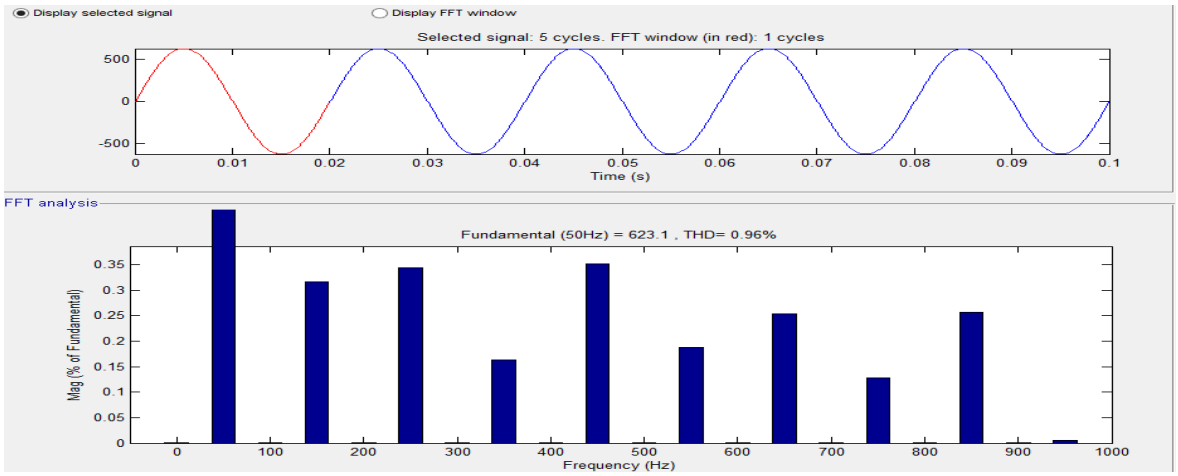

Figure 5. FFT analysis of Total harmonic distortion 0.96% of single phase proposed MLI topology

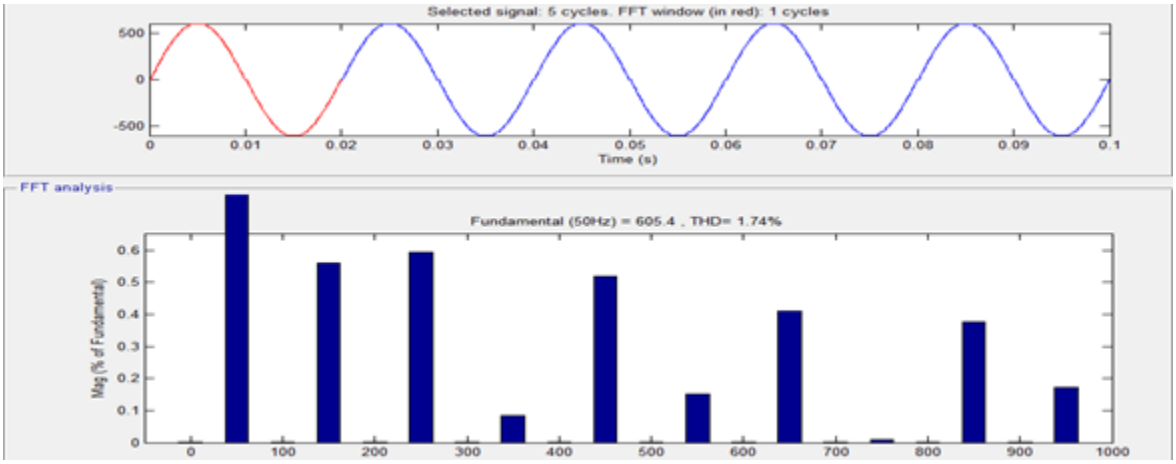

Figure 6. FFT analysis of Total harmonic distortion 1.74% of single phase classical MLI topology

Table 3. Comparison Table between Single Phase Classical and proposed MLIs

Topology	Number of DC sources	Number of switches	Switching losses (%)	Fundamental Voltage	THD (%) of V_{out}
Classical 127 level MLI	6	24	X(assumed)	605.4v	1.74
Proposed 127 level MLI	6	16	0.66X	623.1v	0.96

4. CONCLUSION

In this paper, a novel basic unit is proposed in proposed cascaded multilevel inverter. If all the basic units are connected in series form then a cascaded multilevel inverter is obtained which produces positive levels only. To get negative levels along with positive levels, an H-bridge is added to the proposed cascaded multilevel inverter. Thus single phase proposed 127 level optimal multilevel inverter is designed with minimum IGBT switches and 6 dc sources when compared to single phase classical 127 multilevel inverter which is designed with more IGBT switches and same dc sources. Therefore switching losses are less in proposed topology than that of classical topology. The proposed MLI topology offers more fundamental voltage and less total harmonic distortion 0.96% when compared to classical MLI topology due to the cause of optimal structure with more number of levels at output causes to produce quality sinusoidal waveform which can applicable for ac motor drives.

REFERENCES

[1] E. Babaei, S. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3932–3939, Aug. 2014.

[2] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of sub-multilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, Feb. 2013.

[3] J. H. Kim, S. K. Sul, and P. N. Enjeti, "A carrier-based PWM method with optimum switching sequence for a multilevel four-leg voltage source inverter," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1239–1248, Jul./Aug. 2008.

[4] O. Lopez *et al.*, "Comparison of a FPGA implementation of two multilevel space vector PWM algorithms," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1537–1547, Apr. 2008.

[5] E. Babaei and S. Sheer mohammad zadeh, "Hybrid multilevel inverter using switched-capacitor units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4614–4621, Sep. 2014.

[6] A. A. Boora, A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "Voltage sharing converter to supply single-phase asymmetric four-level diode clamped inverter with high power factor loads," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2507–2520, Oct. 2010.

[7] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on natural point clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[8] E. Babaei, M. F. Kangarlu, M. Sabahi, and M. R. Alizadeh Pahlavani, "Cascaded multilevel inverter using sub-multilevel cells," *Electr. Power Syst. Res.*, vol. 96, pp. 101–110, Mar. 2013.

[9] J. C. Wu, K. D. Wu, H. L. Jou, and S. T. Xiao, "Diode-clamped multilevel power converter with a zero-sequence current loop for three-phase three-wire hybrid power filter," *Elect. Power Syst. Res.*, vol. 81, no. 2, pp. 263–270, Feb. 2011.

[10] N. Farokhnia, S. H. Fathi, N. Yousefpoor, and M. K. Bakhshizadeh, "Minimizations of total harmonic distortion in cascaded multilevel inverter by regulating of voltages DC sources," *IET Power Electron.*, vol. 5, no. 1, pp. 106–114, Jan. 2012.

[11] S. Laali, K. Abbaszadeh, and H. Lesani, "Control of asymmetric cascaded multilevel inverters based on charge balance control methods," *Int. Rev. Elect. Eng.*, vol. 6, no. 2, pp. 522–528, Mar./Apr. 2011.

[12] E. Babaei and S. H. Hosseini, "Charge balance control methods for asymmetrical cascade multilevel converters," in *Proc. ICEMS*, Seoul, Korea, 2007, pp. 74–79.

[13] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel DC voltage sources," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2643–2650, Aug. 2010.

[14] Thiyagarajan V, Somasundaram P"A New Seven Level Symmetrical Inverter with Reduced Switch Count" International Journal of Power Electronics and Drive System (IJPEDS) Vol. 9, No. 2, June 2018, pp. 921~925

[15] Lipika Nanda, A Dasgupta, U. K. Rout "A comparative Analysis of Symmetrical and Asymmetrical Cascaded Multilevel Inverter Having Reduced Number of Switches and DC Sources" International Journal of Power Electronics and Drive System (IJPEDS) Vol. 8, No. 4, December 2017, pp. 1595~1602

[16] Aparna Prayag, Sanjay Bodkhe "Novel Symmetric and Asymmetric Multilevel Inverter Topology for Permanent Magnet Synchronous Motor" International Journal of Power Electronics and Drive System (IJPEDS) Vol. 8, No. 3, September 2017, pp. 1002~1010.

[17] Suroso, Abdullah Nur Aziz, Toshihiko Noguchi "Five-level PWM Inverter with a Single DC Power Source for DC-AC Power Conversion" International Journal of Power Electronics and Drive System (IJPEDS Vol. 8, No. 3, September 2017, pp. 1230~1237

[18] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *J. Energy Convers. Manage.*, vol. 50, no. 11, pp. 2761–2767, Nov. 2009.

[19] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. Tarafdar Haque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," *Elect. Power Syst. Res.*, vol. 77, no. 8, pp. 1073–1085, Jun. 2007.

[20] S. Laali, K. Abbaszades, and H. Lesani, "A new algorithm to determine the magnitudes of DC voltage sources in asymmetrical cascaded multilevel converters capable of using charge balance control methods," in *Proc. ICEMS*, Incheon, Korea, 2010, pp. 56–61.

BIOGRAPHIES OF AUTHORS

B. Madhusudana Reddy is currently a Research Scholar at Jawaharlal Nehru Technological University, Anantapur, Andhra Pradesh, India. He received his B.Tech Degree in Electrical and Electronics Engineering from Jawaharlal Nehru Technological University, Hyderabad, Andhra Pradesh, India and M.Tech Degree from Jawaharlal Nehru Technological University, Hyderabad, India. His current research is focused on multilevel inverters fed induction motor using different controllers.

Dr. Y. V. Siva Reddy is currently working as Professor, Board of Studies Member and Director of Research and Development at G.PullaReddy Engineering College, Kurnool, Andhra Pradesh, India. He received his B.Tech Degree in Electrical and Electronics Engineering from Jawaharlal Nehru Technological University, Hyderabad, Andhra Pradesh, India and M.Tech Degree from Jawaharlal Nehru Technological University, Hyderabad, India and Ph.D Degree at Jawaharlal Nehru Technological University, Anantapur, Andhra Pradesh, India. His area of interest is Power Systems and Electrical Drives. He has been published more than 25 research papers.

Dr.M.Vijaya Kumar is currently working as Professor in the department Electrical and Electronics Engineering, JNT University, Anantapur, Andhra Pradesh, India and Director of Academics and planning, JNTUA, Anantapur, India. He graduated from NBKR Institute of Science and Technology, Vidyanagar, A.P, India, M.Tech degree from Regional Engineering College, Warangal, India and Ph.D from JNT University, Hyderabad, India in 2000. He is a member of Board of studies of and JNT University, Anantapur, A.P, India. He has been published more than 50 research papers. He received two research awards from the Institution of Engineers (India) and also received best teacher award in 2015 from State government of A.P. His areas of interests include Electrical Machines, Electrical Drives, Microprocessors and Instrumentation.