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Enhanced Zeta Converter for DC Bus Voltage Regulation

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ABSTRACT

In this paper, an Enhanced Zeta Converter (EZC) along with a high voltage gain converter is presented for DC Bus voltage regulation. The enhanced zeta converter consists of capacitors connected in parallel with the conventional zeta structure. The proposed zeta converter is applied to the Photo Voltaic system (PV) The well known Maximum Power Point Tracking (MPPT) P & O algorithm is used to extract maximum power from the photovoltaic system. The increased voltage is obtained with reduced number of switches using the proposed structure. The results to the proposed structure are compared with the conventional topology. The proposed converter is simulated using MATLAB and the same is verified with the hardware.

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1. INTRODUCTION

Electricity plays a vital role in our day to day life and the generation of electricity using fossil fuel will be available for a short duration only as the resources are vanishing. The alternate solution for power generation is done by renewable sources so that the demand of electricity can be met. The sources available in nature could be used as the compensation of energy demand. In that, the energy from Sun in the form of irradiation is converted into electrical energy and can be connected to the grid. This conversion is done by PhotoVoltaic (PV) arrays[1]. But only with the help of PV arrays the fruitful result cannot be achieved as the output voltage is very low. So power electronic components are utilized to increase, decrease or the voltage levels. There are some types of boost converters[8] which can regulate the output voltage. Even though, the output voltage could not be increased beyond a certain level. Normally boost converters are used for increasing the voltage that operates at high duty ratio. However due to loss of power, loss in switching and Equivalent Series Resistance of inductors (ESR), capacitors, the overall efficiency is pulled down[2].

To overcome these limitations zeta converters are used because zeta converter is one of the buck-boost converters. But due to switching losses, diodes resistors, inductors and capacitors the gain of the system still fails[3-4].To overcome these limitations of the boost converters, various other converters like interleaved boost converters, soft switching boost converters, structure of coupled inductors and voltage multiplier circuits using capacitors were used for getting high gain compared with the conventional methods. But every converters have some of advantages and disadvantages.

The main disadvantage of soft switching boost converter is its complexity in structure and usage of more number of components. These converters operate in Zero Voltage Switching (ZVS) mode that give rise to reduction of losses created by switches and increased efficiency. For succeeding to get high voltage gain voltage multipliers are incorporated with the converters. A typical voltage multiplier has fixed inputs and voltage ratio. The major advantage of using these multipliers are that they are less in weight, smaller in size, high in power density, high efficiency and most importantly less in magnetic structure. With this arrangement of components, the output voltage of the circuit can not give the regulated output because the circuit mainly depends on the input voltage. These are also use more number of power electronic switches which in turn increases the cost and the size of the circuits. This reflects in non utilization of Maximum Power Point Tracking (MPPT) in Photovoltaic systems [5].

Recently more number of voltage multiplier converter topologies are presented yielding in the usage of larger number of capacitors and controllers. An existing voltage multiplier converter[6] topology with multilevel flying capacitor DC-DC converter has n capacitors and 2n switches. The amount of generated output DC voltage for any given input voltage (V_{in}) is nV_{in}[6]. It is to be noted that for increasing the output voltage, the inclusion of power switches will be increased. Added to that, the output voltage cannot be regulated.Another voltage multiplier [9] also available in which the number of switches for n capacitors are 3n whose output voltage can be calculated by $(n+1)V_{in}$. The output current got from this topology is discontinuous. The major disadvantage of using this topology gives an unregulated output voltage and so these topologies are not used for PV application due to its limited tracking of maximum power point. In this paper a new enhanced zeta converter with high voltage gain for PV application is presented. This can overcome the drawbacks found in the conventional topologies. Here both simulated and experimental results are added to verify the performance of proposed topology.

2. PROPOSED ENHANCED ZETA CONVERTER

The structure of the proposed system has two stages. The first stage being the conventional zeta and the second stage is of high voltage gain converter. The second stage of the proposed system is consisting of n charging capacitors $C_1, C_2, \ldots C_n$ and the controlling switches $T_1, T_2, \ldots T_n$. it is also has the 2n power diodes $D_{a1}, D_{a2}, \ldots D_{an}$ and $D_{b1}, D_{b2}, \ldots D_{bn}$. The first stage which has DC voltage source (Vin) and two inductors (L_1, L_2), the capacitors (C_{n+1}, C_o), a diode (D_{n+1}) and one switch T_1. The main disadvantage of the normal zeta converters are

a. It has low limited voltage gain.
b. Gives a discontinuous input current

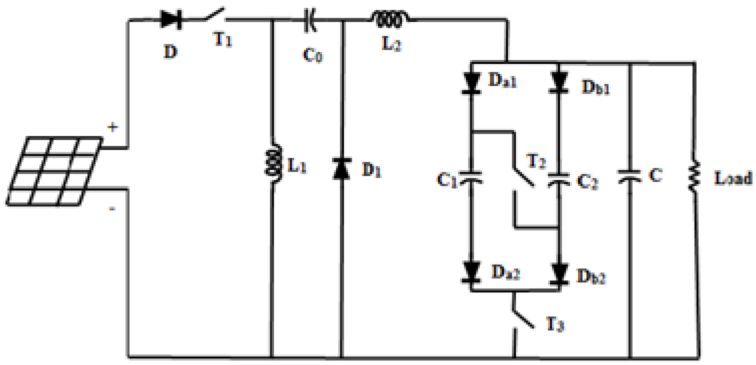

Figure 1. Proposed Enhanced Zeta Converter

The major disadvantages of high voltage gain [8] converters:

a. Gives a discontinuous input current.
b. Difficult to regulate the output voltage.
c. It cannot be suitable for PV applications.

To overcome the above said disadvantages the proposed enhanced zeta converter is designed. It has the following advantages

a. The gain of the design is increased.
b. The voltage regulation can be achieved by properly adjusting the duty cycle.
c. It can also track Maximum Power when it is used for PV application.
d. Gives reduced cost.
e. Gives less loss as number of switches are less.
f. The proposed design gives a continuous input current.

3. MODES OF OPERATION

Mode I:

In this mode, switch T_1 is closed and the switches T_2,T_3,…T_n are also closed. The diodes D_{a1},D_{a2},..D_{an} and D_{b1},D_{b2},…D_{bn} are turns ON. Now the input to the zeta is V_s and the output of the (V_s) of the first stage is the voltage across the capacitor V_{co}. This V_{co} is applied to the second stage. Here the capaciors connected in series are getting charged and the output voltage of the second stage V_{out} is the sum of the voltages in inductor L_1 ,L_2 and the voltage across the capacitors V_{C1},V_{c2}….Vcn as shown in Figure 2.

Mode II:

In this mode, the switches T_2,T_3,…Tn are closed and the switch T_1 is open. The diodes Da_1,Da_2,…D_{an} and D_{b1},D_{b2},….D_{bn} are turned ON. At this stage, the capacitors C_{n+1} and the inductors L_1 and L_2 is discharging and giving a voltage V_o which is fed to the parallel capacitors as shown in Figure 3.

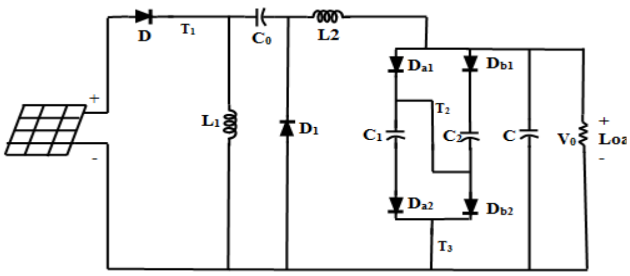

Figure 2. Modes of operation (Mode I)

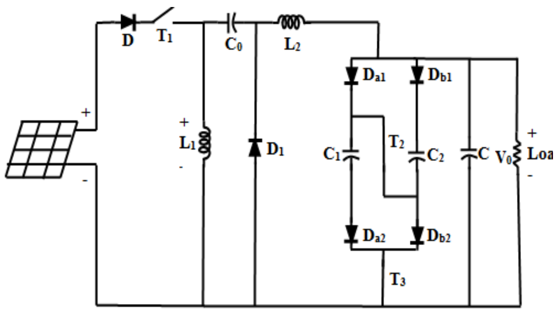

Figure 3. Modes of operation (Mode II)

4. DESIGN OF ENHANCED ZETA CONVERTER

This section gives the design of important components like inductor, capacitor and diodes and the total voltage gain [9]and losses are calculated in this section. Figure 4 illustrates the steady state current waveforms of i_{L1},i_{L2},i_{in},i_{cn+1},i_{c0} and V_{c0} in one switching cycle. These are useful for calculating the main parameters. Calculation of voltage gain. The average voltages across the inductor at the charging and discharging time period Tin the steady state operation will be equal to zero. Then

$$\int_0^T VL_2 = \int_0^{DT} V_S + VC_{n+1} - V_o + \int_T^{(1-D)T} (-V_0)di \quad (1)$$

$$V_S D + V_{cn+1}.D - V_0 = 0 \quad (2)$$

The output V_0 can be written as

$$Vs = \frac{D}{(1-D)}.V_{in} \quad (3)$$

The output voltage of enhanced high gain converter can be calculated as

$$V_0 = (n+1)V_S \quad (4)$$

where n represents the number of capacitors.

By Equations (3) and (4), the voltage gain of the proposed topology is given by

$$V_0 = \frac{(n+1)D}{(1-D)}V_{in} \quad (5)$$

Here $D = \frac{Ton}{T}$ is the duty ratio of switches (6)

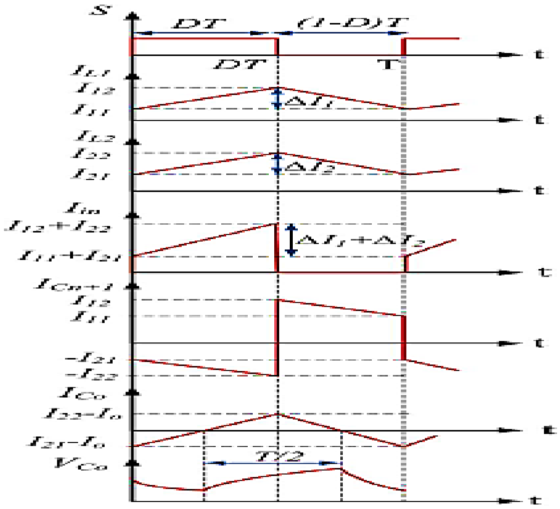

Figure 4. Waveforms of proposed enhanced zeta

4.1. Calculation of Inductor and capacitor

In this chapter, the values of inductors (L_1,L_2,L_3,..L_n) and capacitors (C_1,C_2,…C_n) are derived to minimize the voltage & current ripples. The calculation of inductor is done by

$$i_{L1}(t) = \frac{1}{L}\int_0^t VL1\,dt + I_{L11} \quad (7)$$

The ripple current in the inductor L_1

$$\Delta I_{L1} = I_{L12} - I_{L11}$$

$$\Delta I_{L1} = \frac{1}{L} V_{L1}\,DT = \frac{Vs}{L1.f} \quad (8)$$

Using the Equations (4) and (8)

$$\Delta I_{L1} = \frac{(n+1)D}{L1f} V_{in} \quad (9)$$

The value of inductor can be found as

$$L_1 = \frac{(n+1)D}{\Delta IL1.f} V_{in} \quad (10)$$

Similarly, $\Delta I_{L2} = I_{L22} - I_{L21} = \frac{(1-D)V0}{L2.f}$ (11)

$$L_2 = \frac{(1-D)V0}{f.\Delta I2} \quad (12)$$

To calculate the values of capacitors (C_1,C_2…C_n), it is obvious that the capacitors are series then the charging currents in all the capacitors are equal ie

$$i_{c1} = i_{c2} = \ldots i_{cn} = -i_c = \frac{-I0}{(1-D)} \quad (13)$$

by knowing thvlues of charging currents, the voltage across the capacitors can be found. Therefore

$$V_{c1} = V_{c2} = .. = V_{cn}$$

$$V_{cn} = \frac{1}{Cn}\int_0^{DT} icn\,dt + V_{cn}(0)$$

$$V_{cn} = \frac{1}{Cn}\int_0^{DT} \frac{I0}{(1-D)}\, dt + V_{cn}(0) \tag{14}$$

By the above Equations it is noted that the voltage ripples of the capacitors, (V_{C1},V_{C2},…V_{Cn}) are equal and the values of capacitors are found using

$$\Delta V_{C1}=\Delta V_{C2}=\Delta V_{Cn}= \frac{V0\ D}{Cn(1-D)fRL} \tag{15}$$

Then we have,

$$C_1=C_2=\ldots C_n = \frac{V0D}{\Delta VCn(1-D)fRL} \tag{16}$$

If the element designed in this topology are considered as ideal, then the input currents (I_{in}) of the proposed topology is given by

$$I_{in} = \frac{(n+1)DI0}{(1-D)} \tag{17}$$

Design ratings of switches. Design of switches play a vital role in the converters because of the cost. The switches are T_1,T_2,…TN and the voltage ratings of the switches are given by (V_{Ti}).

$$V_{Ti} = n.V_{in} \qquad i=1,2,3\ldots n \tag{18}$$

$$V_{T1} = n.V_{in} \tag{19}$$

But for the voltage rating of the switch used in Zeta converter is given by

$$V_{T\ n+1} = \frac{1+nD}{1-D}V_{in} \tag{20}$$

Now from the Equations (18), (19) & (20), we can get the total voltage of the proposed topology as

$$V_{Ti} + V_{Ti'} + V_{T\ n+1} = (2n + \frac{1+nD}{1-D}V_{in}) \tag{21}$$

4.2. Calculation of Losses

In all the existing converters, the losses created by the switches are present. We know that there are two types of losses namely conduction loss and switching loss. Moreover other losses like loss in diodes and capacitance loss is also there. So we need to calculate the total loss ie conduction loss and switching loss which are mainly depend on the voltage values.

$$P_{cs} = V_1 I_{av} + Rs.I_{rms}^2 \tag{22}$$

Added to the above losses, the switching losses are to be calculated. The loss is computed as

$$P_{sw,s} = f.[\int_0^{ton} Vs.Is + \int_0^{toff} Vs.Is'dt \tag{23}$$

Here V_s,I_s and I_s' give the value of blocked volage, switching current during first mode and switching currents during second mode. Using these two losses, the total loss is calculated by

$$P_{sw} = P_{sw}T_1' + P_{sw},T1 + \sum_{i=1}^{n} Psw1\ Ti \tag{24}$$

Where the parameters Psw,Ti',Psw, T1 and $\sum_{i=1}^{n} Psw1\ Ti$ are denoting the switching losses Tn' T1 and charging switches respectively. These values are determined by

$$\sum_{i=1}^{N} Psw,Ti = \frac{VinVof}{6RL(1-D)}(t_{on}-t_{off}) \tag{25}$$

$$P_{sw},T_1' = \frac{VinVofDn2}{6RL(1-D)}(t_{on}-t_{off}) \tag{26}$$

$$P_{sw},T1= \frac{(1+nD)vinVof}{6RL(1-D)2}\,(t_{on}-t_{off}) \quad (27)$$

Therefore the total loss (P_{loss}) is

$$P_{loss}= P_{sw}+ P_c \quad (28)$$

5. SIMULATION AND EXPERIMENTAL RESULTS

The Figure 5 and Figure 6 show the simulation diagram and its output of the conventional zeta converter. Here the output voltage is boosted up to 210V for an input voltage of 25V.

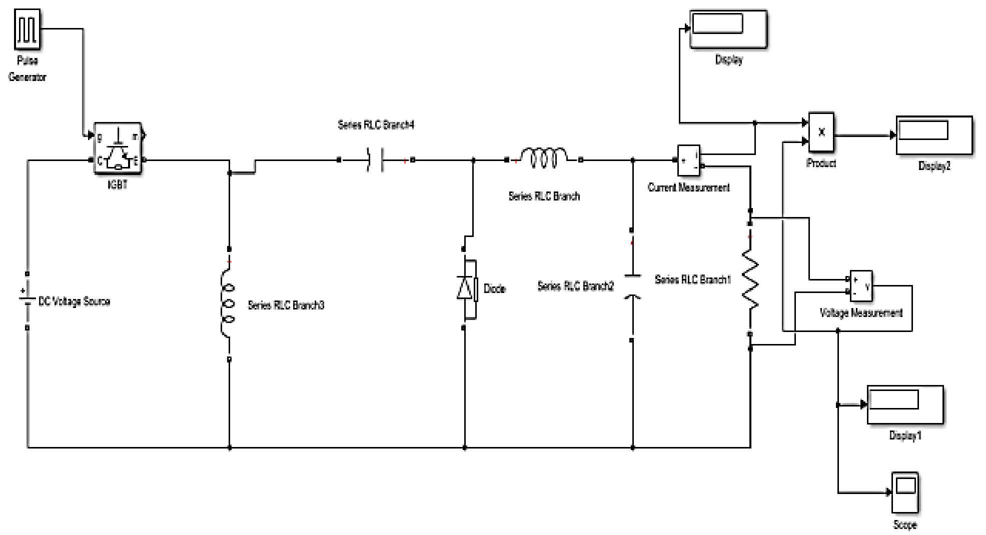

Figure 5. Simulation diagram of existing zeta converter

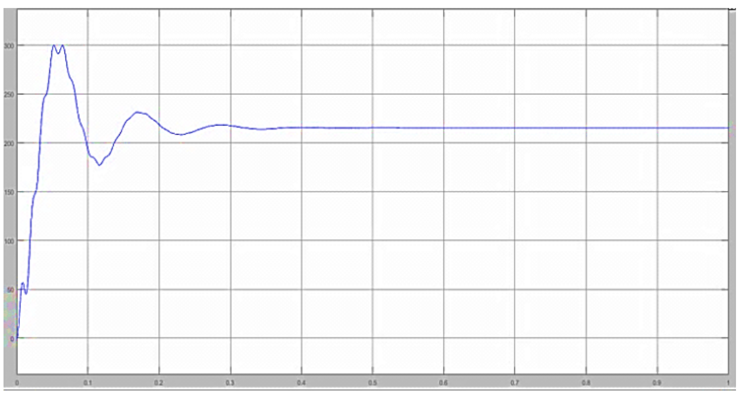

Figure 6. Existing zeta converter in boost mode (voltage output)

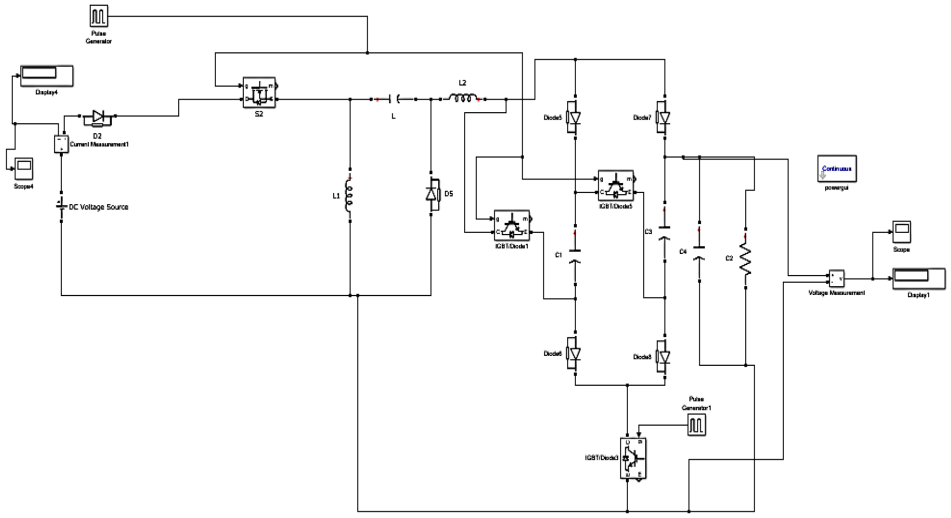

Figure 7. Simulation diagram of proposed system

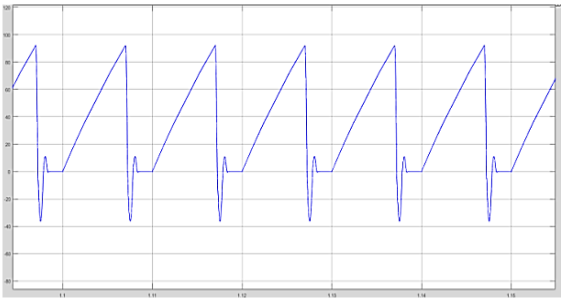

Figure 8. Current through the inductor 1(L_1)in proposed work

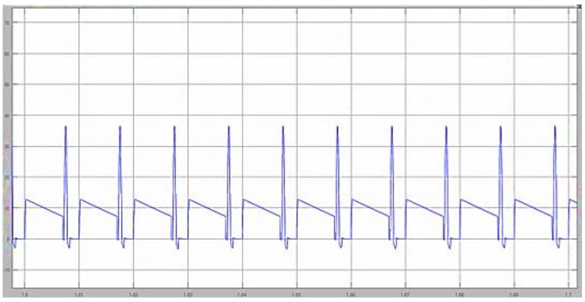

Figure 9. Current through inductor 2(L_2)

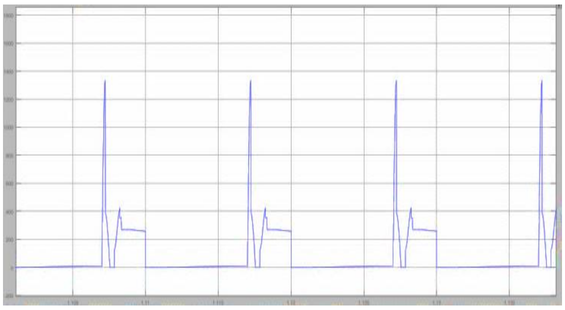

Figure 10. Blocked voltages by switch T_1

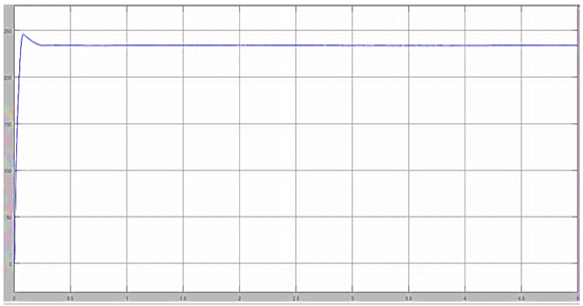

Figure 11. Simulation results for output voltage

The output voltage obtained for the zeta converter [7] is 210 V, whereas for the same rating for the proposed zeta converter the output voltage is 240V. So the output voltage is increased by 30V which is approximately 13% increment in input voltage. The total losses for the porposed converter are 10W so the efficiency of the converter is 94%. Thus the proposed converter can maintain the output voltage for the load variation to 13%. To justify the advantages of the proposed structure, the performance is explained by assuming n=2. The experimental setup is done which is indicated in Figure 12. The power electronics components used for the experimental setup is given in the Table 1.

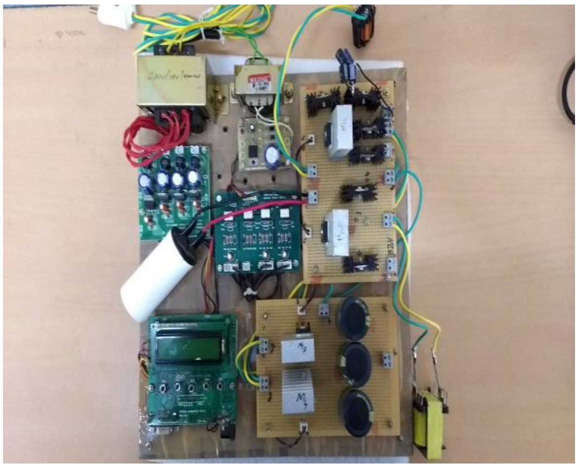

Figure 12. Hardware set up of proposed work

Table 1. Experimental Parameters

Component	Type	Quantity
Inductors	0.57 mH/10 A	2
Capacitors	12.5 MFD, 440 VAC, 50 Hz	1
	4700 μF, 100 W	3
	100 μF, 50 V	4
MOSFET	IR250	4
Power Diodes	BYQ28	6

The performance of the enhanced zeta converter is compared [7]with other converters which is given in the Table 2. From the comparison it is evident that the cost of the proposed converter is low, number if switches are less. Also the voltage gain is high compared to other converters.

Table 2 Comparison of proposed topology with other similar topologies

Type of topology	Multilevel DC – DC Converter	Switched Capacitor High voltage gain boost converter	Switched capacitor With reduced number of switches	Enhanced zeta converter.
Cost	Average	Average	High	Low
Output voltage	Non variable	Non variable	Non variable	Variable
System gain	nV_{in}	$(n+1)V_{in}$	nV_{in}	$\frac{(n+1)D}{(1-D)} V_{in}$
MPPT	No	No	No	Yes
Number of switches	2n	3n	2n	N+1
Number of capacitor	n+1	n	n+1	n

6. CONCLUSION

In this work an enhanced zeta converter was presented. The various modes of operation of the proposed structure is done. The output voltage gain of the proposed sytem depicts that for a reduced input voltage the output is increased by13% than existing system. So the load voltage can be regulated for a variation of 13%. The proposed converter has various benefits like less number of switches, less number of capacitors and less cost.

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