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# Comparative Analysis of Different PWM Techniques to Reduce the Common Mode Voltage in Three-Level Neutral-Point-Clamped Inverters for Variable Speed Induction Drives

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**ABSTRACT**

This work presents the comparative study of the different PWM techniques to reduce the common-mode voltage (CMV) at the output of neutral point diode clamped inverter for variable speed drives. Here the comparative study is done by the phase opposition disposed (POD), sinusoidal pulse width modulation (SPWM), phase disposition (PD), phase shift (PS) space vector modulation (SVM) techniques are proposed. A good trade-off between the quality of the output voltage and the partial magnitude of the CMV is achieved in this work. The scheme is proposed for three-level inverter. This work realizes the implementation of Three-level diode clamped MLI for three-phase (Y-Δ) induction motor with the implementation of a space vector modulation technique without any additional control algorithm to reduce CMV within the range $\pm V_{dc}/6$. The Simulation with a 1HP induction motor drive system is setup in Matlab-2011b and the same results validated effectively by hardware – FPGA-SPARTEN III processor and its shows that the CM voltage is effectively reduced and the maximum output voltage is not affected.



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## 1. INTRODUCTION

Inverters are widely used in various industrial applications such as power conditioning system for renewable energy and variable speed drives system because of their ability to control the magnitude and frequency of the output voltage [15] [16]. Recently, to reduce the harmonics in the inverter output voltage and to meet the voltage rating of the power devices the multi-level structures are used. Multilevel inverters have been more advantages, due to its performance like power ratings, improved harmonic performance and reduced EMI emission that can be achieved with the multiple DC levels that are available for synthesis of the output voltage waveforms [2] [14]. The multilevel inverter consist of three topologies that are diode-clamped (DC-MLI), capacitor-clamped inverters (FC-MLI), and cascaded inverters (H-bridge-MLI) [14] [16] [2]. The inverters, has a various types of modulation strategies that have been used as the control the performance of the inverter. The most popular PWM techniques are carrier-based and Space Vector Modulation (SVM) [14] [2]. Carrier-based modulation strategies have two types that are single carrier and multi carrier PWM. The

diode clamped inverters have some advance features like stair case waveform; reduced harmonics and it have attractive features of controlling the medium voltage drives [21] [14].

For diode-clamped inverters the carrier based modulation techniques like PD (phase disposition), POD (phase opposition disposition), APOD (Alternative phase opposition disposition), PS (phase-shift) are well suited [4] [13]. For Diode clamped inverters, Phase opposition disposition (POD) carrier-based modulation strategies are the most widely used but it offer high harmonic performance [1]. From the two modulation schemes the SVPWM scheme gives the high fundamental output voltage and improved harmonic performance of the inverter [4].

The major applications of NPC can be classified into two broad areas, they are:

Large Motor Drives: Speed control of induction motor, Stator voltage control, direct torque control, V/f control, Rotor resistance control, Slip power recovery scheme [15] [17].

Power Systems Applications: STATCOM, UPFC, power quality, power conditioners, reactive power compensator, grid connected systems etc [14] [16].

More recently MLIs have been used for an increasingly a variety of applications which includes induction machine and motor drives, active rectifiers, filters, interface of renewable energy sources, flexible AC transmission systems (FACTS), and static compensators. NPC MLI‘s are highly robust and highly flexible system [14].

In the applications of AC motor drives, the analysis of the common mode voltage is important. It is produces between the neutral point of the star connected motor (node n) to the earth ground (node e), it leads to common mode current. The CMV is responsible for shaft voltage and premature failure of bearing. The simultaneous switching of the series connected devices generates voltage with a high dv/dt at the output terminal of the inverter. The sudden rise in the inverter output voltage and a long cable are potentially hazardous for the motor insulation and the cable itself. In motor drive applications, it may lead to electromagnetic inference (EMI) noise that causes a nuisance trip of the inverter drive [8] [1]. It is very important to reduce the CMV and limit this voltage within certain bounds. A MLI can reduce as well as eliminate the CMV. Multilevel inverters have a high number of switching states so that the output voltage is stepped in smaller increments [2]. This allows mitigation of the harmonics at low switching frequencies thereby reducing switching losses [14]. Further, the leakage current is reduced because of the lower dv/dt [20]. The cascaded H-bridge multilevel inverter presented in the literature has been implemented successfully in industrial applications for high power drives [6] [12]. However, the drawback is that these inverters need a large number of dc sources or isolation transformers on the ac side. Among the configurations, the analysis of the common mode voltage (CMV) is derived for the NPC inverters, which are the most common configurations of 3-level inverters; because it is most suitable for high and medium voltage drives which are directly connected to the utility power system. They have the single DC source and neutral point of the DC-link tied to each inverter arm by clamping diodes [21]

Several modulation techniques are presented to achieve the reduction in the CMV. Reduction in the CMV have been reported for both carrier-based and SVM schemes. For the CMV reduction issue include multi leg inverter [18], passive filters [8], passive element with active circuitry. Gopakumar et al proposed a scheme whereby CMV cancellation in open end winding motor with excellent performance is shown in [12]–[5]. This configuration is suitable for open end winding motor and requires two three-phase two-level or/and three-level inverters with high rating devices or more dc sources. The retrofitting is not possible with this configuration. Mohan M.Rangeet al [1] has been compared CMV generation with Various SPWM methods like PD, POD, APOD verses carrier reductions, but due to this PWM technique the harmonics are generated in the inverter. In paper [2] Common mode voltage is eliminated partial and also author is mention the schemes are proposed for low switching frequency and more than 5 levels.

The PWM techniques produce different values of CMV in the inverter. In a three-level inverter is used to eliminate CMV but the levels of the phase voltages of the star connected load are reduced from five to three and the magnitude of the line voltage transition increases [6]-[2]. The same source also reported that the tradeoff between the magnitude of the CMV and the switching states gives rise to lower order harmonics in the phase voltage. In this paper CMV reduction is proposed using the space vector modulation (SVM) technique. A three level diode clamped multilevel inverter is fabricated for a three-phase, 3 hp, 400 V induction motor (Figure 1). Sinusoidal PWM, PD-SPWM, POD-SPWM, PS-SPWM, SVM techniques are implemented using a Matlab-2011b For a switching frequency of 1050 Hz and a modulating index, ma =0:9; The Partial elimination of CMV using space vector PWM (SVPWM) switching schemes are implemented using FPGA-SPARTEN III Processor. Simulation and results are provided to validate the implement of the three-level diode clamped inverter.

## 2. EFFECT OF HIGH CMV

The common mode voltage is measured between the input of the voltage source rectifier to the star connected load. It is defined as [1]

$$\mathbf{V_{NG} = (V_{AN} + V_{BN} + V_{CN})/3}$$

Modern PWM inverters generate high frequency, high amplitude common mode voltages, which induce 'shaft voltage' on the rotor side. When the induced shaft voltage exceeds the breakdown voltage of the lubricant in the bearings, result in large bearing currents [17]. The common mode voltage leads to common mode current in the system.Its leads malfunctioning of sensitive electronics & control Systems [5][6].The common mode currents can cause problems such as false tripping of the ground fault relays.This damages the bearings, leading to motor failures and also causes EMI [4]. Since the motor line to line terminal voltage must be either + Vdc or. -Vdc, it is not possible to have the average three terminal voltages to be a zero at any instant of time. The average voltage applied to the motor (over a cycle) is kept zero, but the instantaneous sum of the voltages at the motor terminals is nonzero. This instantaneous voltage sum is called the common mode voltage [10].

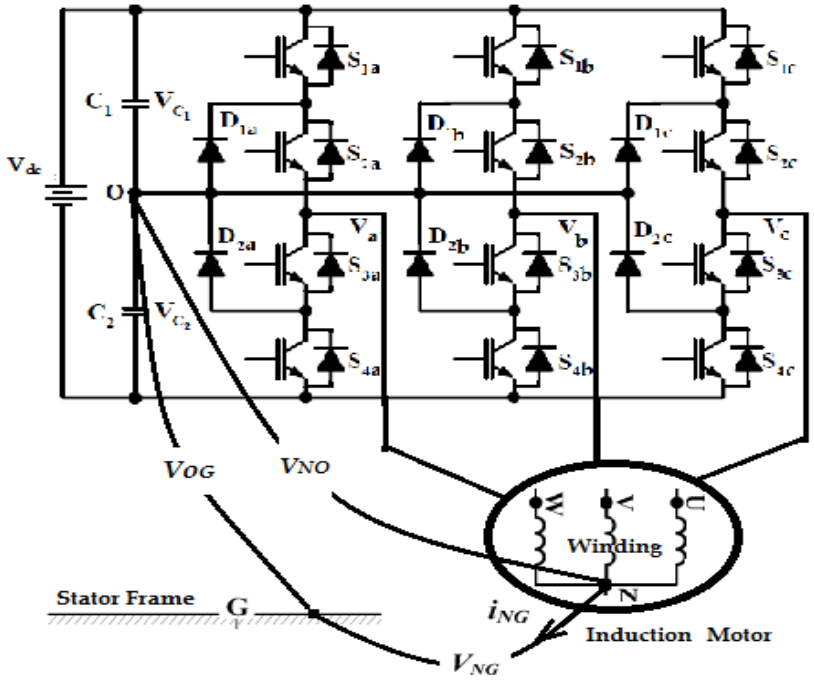



Figure 1. Circuit diagram of three-level NPC induction motor drive with Induction Motor CMV

It can be measured by creating an artificial Y connection at the motor terminals using three large resistors (Mega ohms). The voltage from the center of this Y to the motor ground is the common mode voltage.This voltage exists between the motor windings and the motor ground. It contains high rates of change of voltage with respect to time (i.e. high dv/dt). The high dv/dt creates frequency content in the common mode voltage in the MHz range. For inverter-driven motors, the common mode voltage circuit becomes important shown in figure 1. Common mode currents (I) are created due to capacitive coupling since I = C dv/dt, where C is the capacitance of the common mode circuit element. There are many potential current paths via this capacitive coupling from the motor stator winding to ground. Most of these paths are normally considered to be insulators; a detailed model of the common mode circuit will be presented later in this paper. For now, the most common current paths will be identified and their impact on bearing damage will be qualified. The challenge is to provide sufficiently low impedance ground connections or alternate conductive paths to ensure that the flow of current is properly channeled away from the bearing.

## 3. MODULATION TECHNIQUES

In the carrier based pulse width modulation the triangle carrier wave is compared with the sine reference wave and PWM signal is generated [13] [16].

### 3.1 Single carrier PWM

SPWM technique is popular modulation technique in the inverter. In the SPWM, a sine reference voltage wave is compared with single triangle carrier waveform to generate gate signals in switching of the power electronics devices [16]. Power dissipation is one of the most problems in medium voltage applications. The fundamental frequency SPWM open loop control method is to minimize the switching losses [2].

### 3.2. Multi carrier PWM

The multi carrier PWM method is only for the multi-level inverter. This method is used to increase the performance of multi-level inverters. The carrier waves are arranged in vertical and horizontal. The vertical carrier distribution techniques are classified into three types they are Phase Dissipation (PD), Phase Opposition Disposition (POD), while horizontal arrangement is known as Phase Shift (PS) control technique[1] [9] [13].

**3.2.1. Phase Disposition (PD):** In the phase dissipation technique uses a multi carrier PWM. The number of carriers depends upon the multi level inverter. The technique employs a carrier (m-1) [4]. All of carriers are in phase disposition (PD, the PD-PWM is more useful for NPC [2].

**3.2.2 Phase Opposition Disposition (POD):** This technique employs a number of carriers (m-1) [5] which are all in phase above and below the zero reference. All of the carriers above the zero reference are in phase, but in opposition to those below (POD) [1].

**3.2.3Phase Shift (PS):** This technique employs a number of carriers (m-l) phase shifted by 90 degree accordingly [14] [2].

### 3.3. Space Vector PWM

An n-level inverter consists of 6(n − 1) controllable power semiconductor switches. The space vector diagram (SVD) of a three-phase voltage source inverter consists of six sectors. Among various modulation techniques for a multilevel inverter, space vector pulse width modulation (SVPWM) is an attractive candidate due to the following merits. It directly uses the control variable given by the control system and identifies each switching vector as a point in complex (α, β) space. It can optimize switching sequences [2] [19]. The space vector diagram of any three-phase n-level inverter consists of six sectors. Each sector consists of $(n-1)^2$ triangles. The tip of the reference vector can be located within any triangle. Each vertex of any triangle represents a switching vector. A switching vector represents one or more switching states depending on its location. There are $n^3$ switching states in the space vector diagram of an n-level inverter [7] [6]. There are six sectors ($S_1$−$S_6$), four triangles ($\Delta_0$−$\Delta_3$) in a sector, and a total of 27 switching states in this space vector diagram as shown in figure 2. As level n increases, the increased number of triangles, switching states, and calculation of on-times adds to the complexity of SVPWM for multilevel inverters.

The space vector modulation treats sinusoidal voltage as constant amplitude vector rotating at constant frequency with reference voltage vector $V_{ref}$, defined by $V^*= |V_{ref}|*e^{jvt}$, rotating around the centre of the space vector (SV) diagram at an angular frequency $\omega= 2\pi f_m$.[7]. Space vector modulation directly controls the system, the vector is identified as a point in complex space of (α, β) using this method the harmonics can be eliminated and fundamental voltage ratios in SVM scheme obtained are better.

$$V * \delta_{S1} + V * \delta_{S2} + V * \delta_{S3} = V *$$

$$\delta_{S1} + \delta_{S2} + \delta_Z = 1$$

$\delta_1$, $\delta_{S2}$ and $\delta_{M1}$ are the calculated duty cycles of the switching vectors.

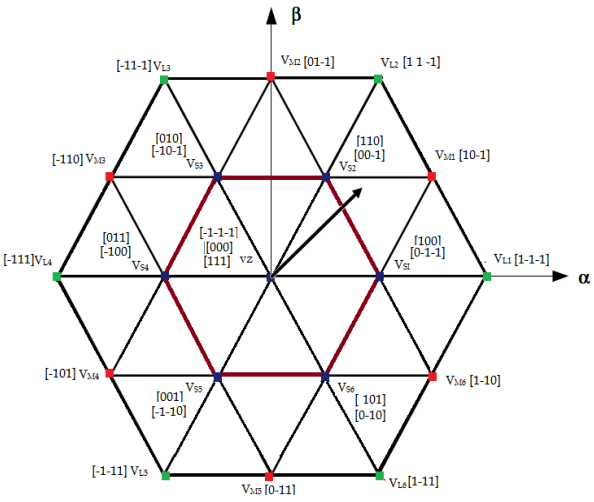



Figure 2. SVPWM for 3-Level NPC Inverter.

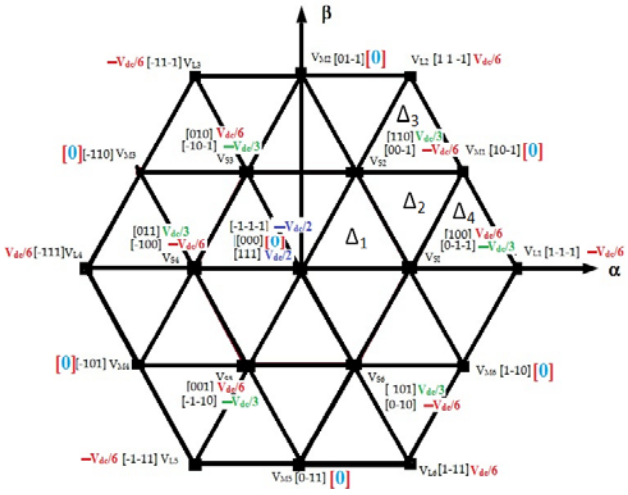


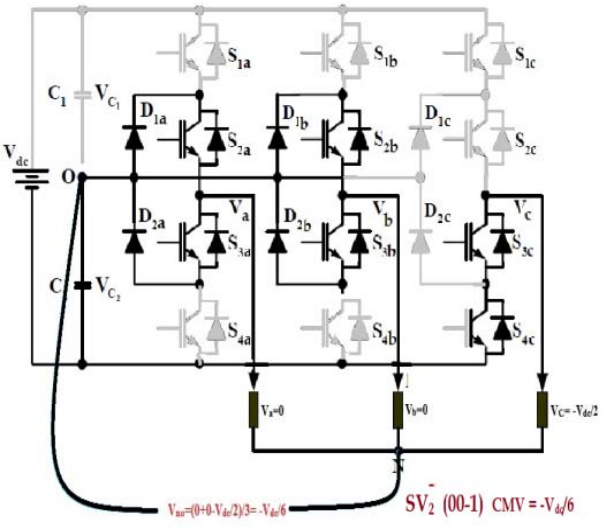

Figure 3. SVPWM Switching states and its CMV

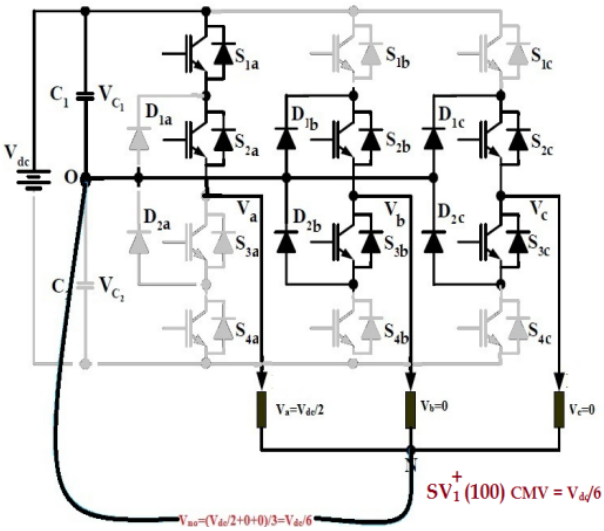
### 3.3.1. ANALYSIS OF CMV DEPEND UPON SWITCHING STATES

The common mode voltage has been discussed for different switching states available in the SVPWM technique. The common mode voltage is defined as the voltage between star connected load neutral point and ground of the inverter. It is given as

$$\mathbf{V_{NG} = (V_{AN} + V_{BN} + V_{CN})/3}$$

The common mode voltage is mostly depend upon the sum of the inverter voltage. In the star connected load sum of the phase voltage must be zero. Here in the 3-level NPC inverter produce different combinations of phase voltages depend upon the switching states available in the SVPWM. In the conventional SVPWM the state 1 produce $+V_{dc}/2$, 0 produces 0V & -1 produce $-V_{dc}/2$. In the operation of the conventional SVPWM has 27 switching states each state has different CMV that has been shown in figure 3 According to the detailed analysis the 12 switching states that produce $\pm V_{dc}/6$, 7 states produce zero CMV, 6 states produce $\pm V_{dc}/3$ & 2 states produce $\pm V_{dc}/2$. The below diagram shows the CMV for triangle $\Delta_0$ in sector 1 with redundant switching states. While operating that triangle the possible common mode voltages are $\pm V_{dc}/2$, 0, $\pm V_{dc}/3$, $\pm V_{dc}/6$ will be obtained.



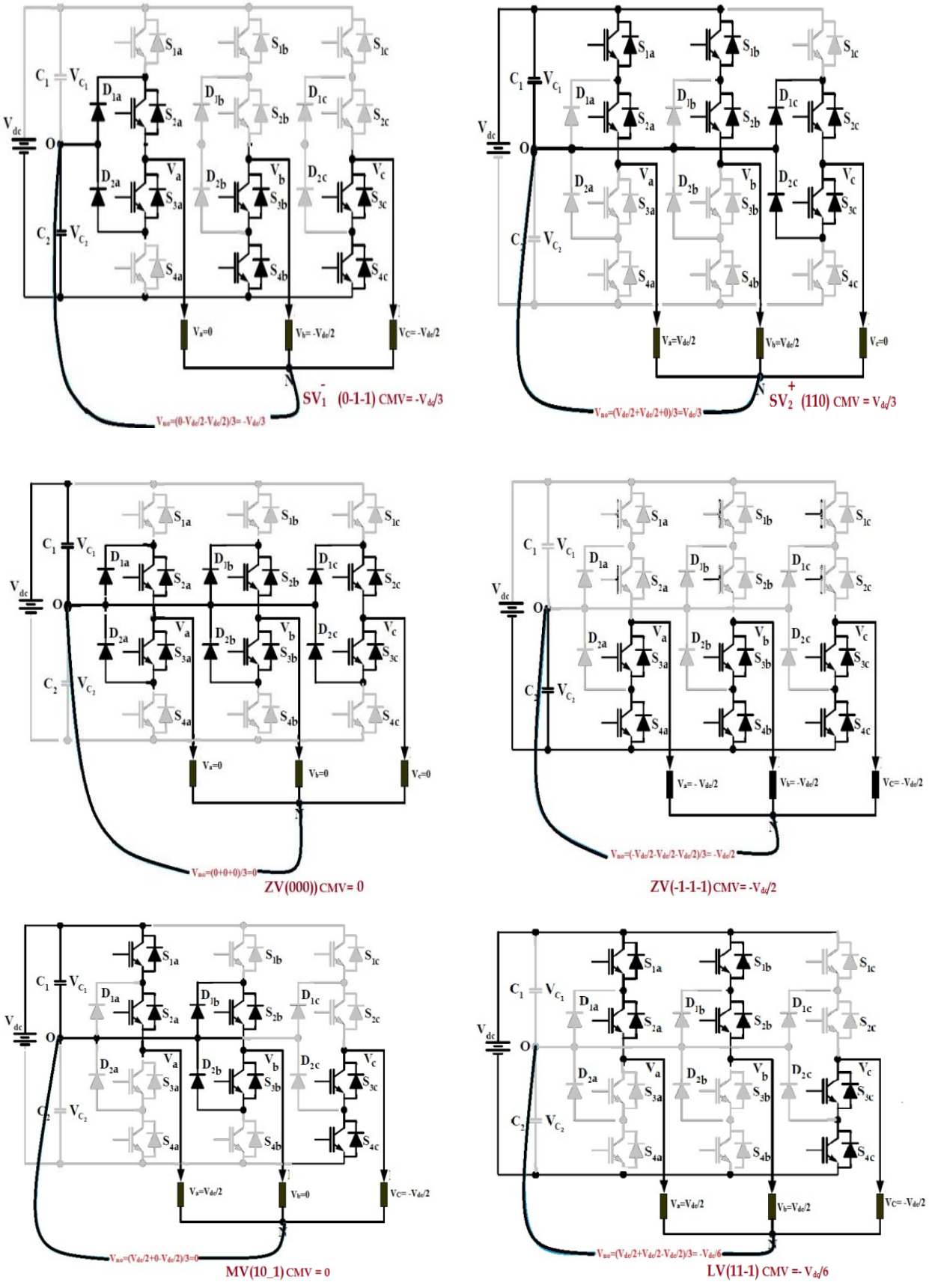



Figure 4. SVPWM Switching states and its CMV

## 4. CMV REDUCTION

The common mode voltage reduction can be done by avoiding abnormal switching of the inverter. The other PWM techniques like PD, APOD, POD, SPWM the controlling the switching operation of inverter is not possible [1] [2]. In SVPWM the controlling of the inverter switching is easy and efficient one. In this paper simple technique is presented to determine the triangle in which the desired vector is located. It is observed that the magnitude of the CMV can be reduced. In this scheme switching Selection can be done using SVPWM without affecting the inverter output voltage. The chapter-3 gives the detailed analysis of the switching states and its common mode voltage. From that analysis by choosing the proper switching states the CMV can be reduced. In the partial elimination the CMV can be reduced up to $V_{dc}/3(n-1)$ for n-level inverter. In the partial elimination the 3-level inverter allows the reduced CMV of magnitude $\pm V_{dc}/6$.

### 4.1. CMV REDUCTION BY SPACE VECTOR MODULATION

In the proposed SVPWM scheme the common mode voltage is reduced to $V_{dc}/6$. In the SVPWM each switching states produce the different values of the common mode voltage (CMV). So common mode voltage is mostly depending upon the sum of zero and short vector [18]. For e.g. zero vector [000] produce CMV zero but another zero vector [111] produces CMV as $V_{dc}/2$. There by choosing the proper switching states in the SVPWM scheme the CMV can be reduced [6] [12]. In the proposed scheme the states which producing the CMV as $\pm V_{dc}/2$, $\pm V_{dc}/3$ can be eliminated. So here the switching schemes are used without redundancy techniques to reduce the CMV up to $\pm V_{dc}/6$. The figure 5 shows the proposed scheme for 3-level SVPWM for 3-level NPC inverter to reduce the CMV. In the proposed SVPWM scheme out of 27 switching states only 19 states are used to obtain CMV as $\pm V_{dc}/6$. With respect to the figure 5 $V_{ref}$ is located in the sector 1 in the triangle $\Delta_0$. At normal operation the switching pulse generated for triangle $\Delta_0$ will consist of three zero vectors (000, 111, -1-1-1), and four short vectors (100, 00-1, 110, 00-1). Due to that CMV value is between $\pm V_{dc}/2$, $\pm V_{dc}/3$, 0 &$\pm V_{dc}/6$. While using the proposed scheme to the triangle $\Delta_0$ it use only one zero vector (000) and two short vectors (100, 00-1) are used because other states in triangle produce CMV value as $\pm V_{dc}/2$ &$\pm V_{dc}/3$. Due to the usage of proper switching states the CMV value is reduced between 0 &$\pm V_{dc}/6$.The Figure 5 shows proposed SVPWM Switching Pulse for Sector 1 in triangle $\Delta_0$ due to that CMV is reduced up to $+V_{dc}/6$. Without using the redundancy technique in the SVPWM the partial elimination of the CMV is obtained.

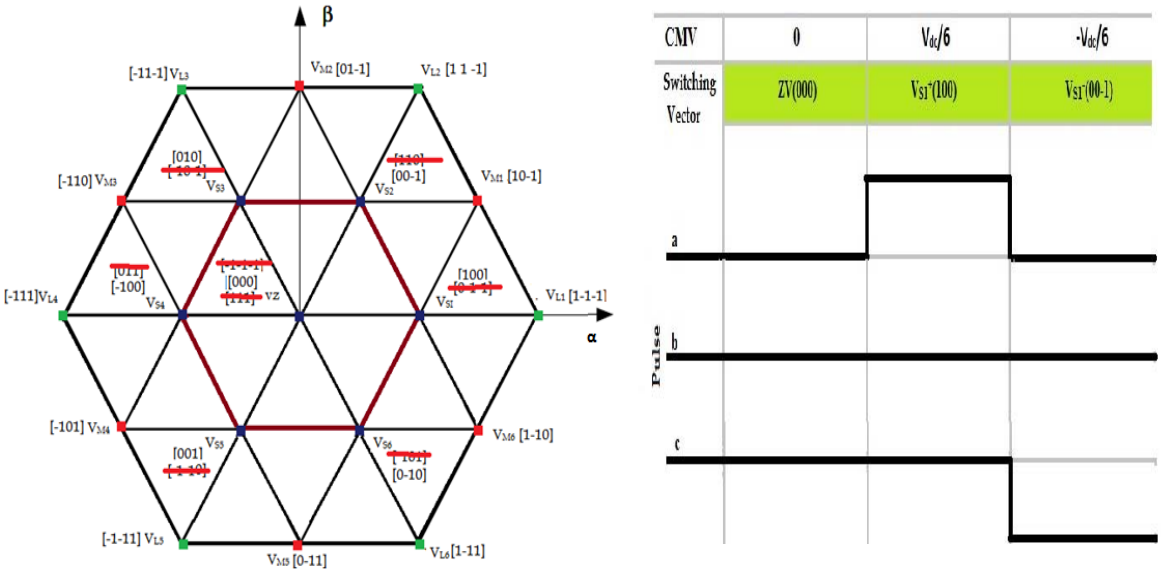
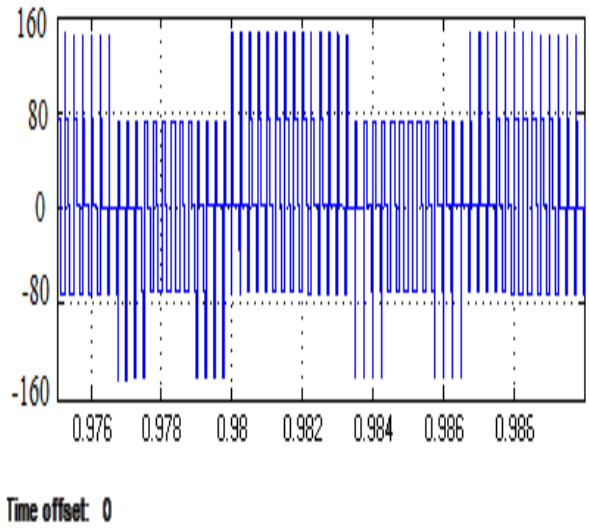



Figure 5. Proposed SVPWM Switching states and its pulse for Sector 1 - $\Delta_0$

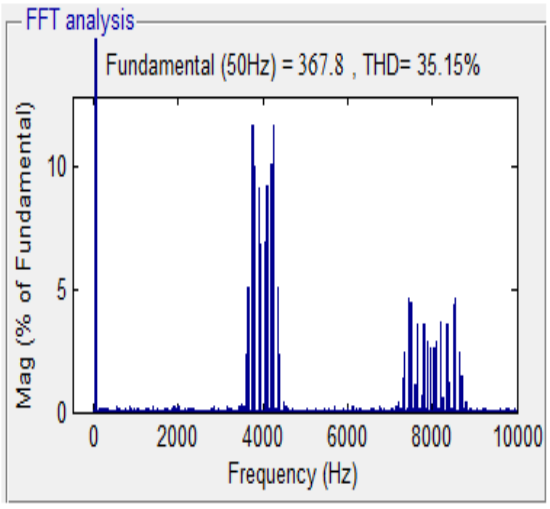
## 5. SIMULATION & EXPERIMENTAL RESULTS

The proposed SVPWM Switching schemes for 3 phase 3 level NPC-MLI Simulation system was setup in mat lab / Simulink, with the system structure is for 2.2Kw, 1440 r/min Induction motor with a rated voltage of 380V & current of 5 A. The Induction motor parameters are stator resistance =2.9 Ω, rotor resistance=2.2Ω, stator leakage induction =12mH, rotor leakage induction=12mH & mutual induction = 290mH. An open loop constant v/f control is used to regulate the motor speed and the DC- link voltage is set at 440 The simulation and experimental result are carried out for 1KHZ switching frequency and modulation

index of 0.877 at 50HZ. The matlab simulation and FPGA based Experimental results are shown the both partial elimination of CMV at neutral point of the motor with respective dc midpoint in figure 9 (a). When the 3-level NPC MLI is controlled by a SPWM techniques are PD, POD & APOD [1]. In this CMV reduced up to $V_{dc}/3$, Vdc/6 &$V_{dc}/6$ respectively. The Simulation results in figure7 Shows that the Common Mode Voltage is reduced up to $V_{dc}/6$ by using proposed Partial elimination SVPWM switching scheme by choosing appropriate Switching state in SVPWM.The 2.2Kw experiential setup is also built to validate the proposed SVPWM schemes to mitigate the Common mode voltage as shown in the figure 9 Which consist of switching module with FPGA developing and Control Board, 3 Phase 3 Level NPC- MLI with 100 micro Farad DC Link capacitors with 3 HP Induction motor load. The control Board is based on FPGA –SPARTEN III family which consist of 1 million gates. The simulation results are closely matching with the experimental results as shown in the Figure 9.




(a)

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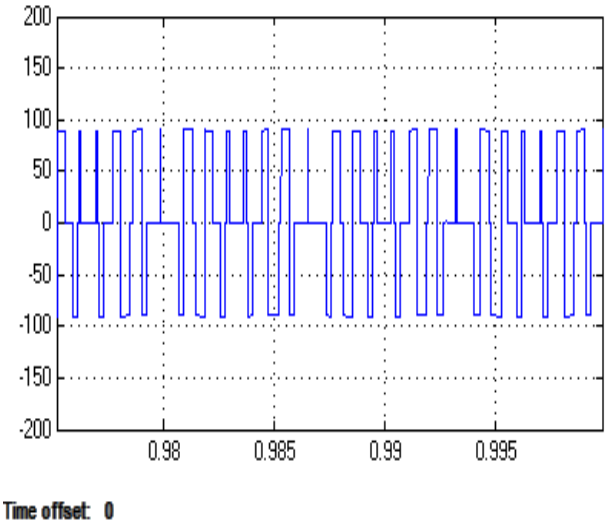


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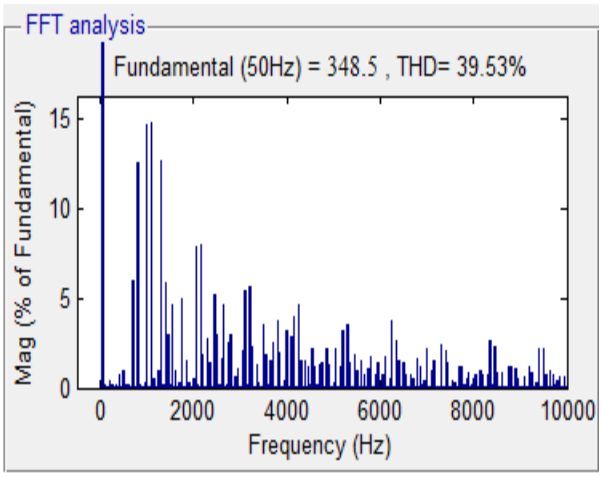
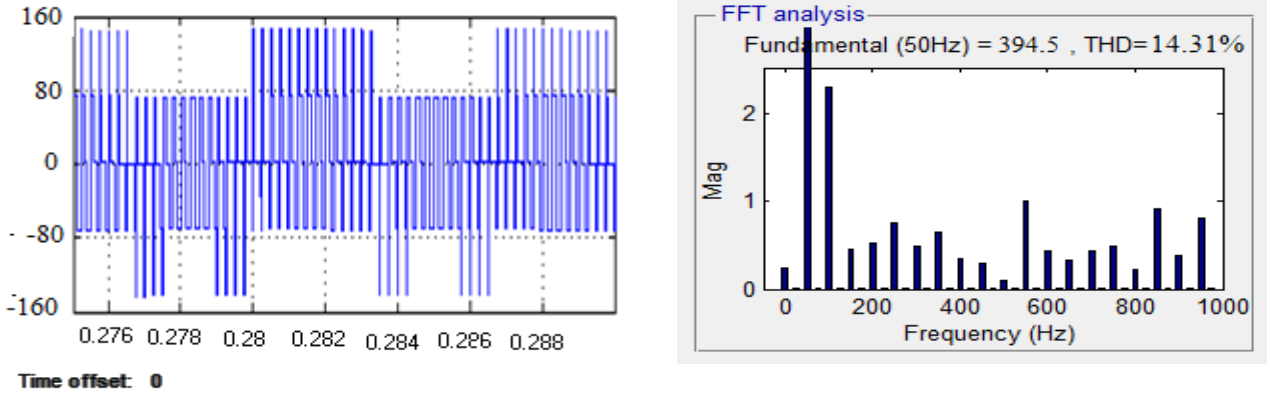
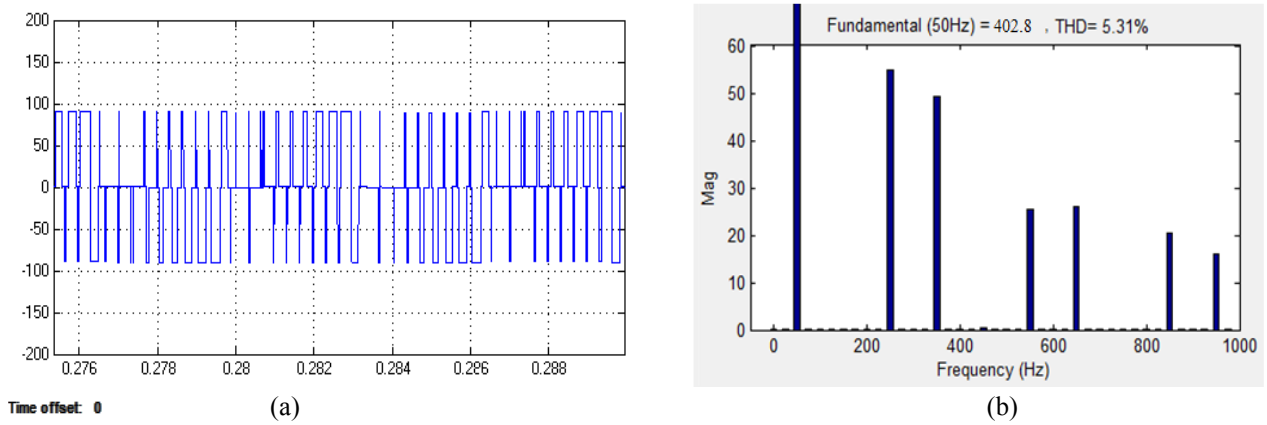



(d)




(e) (f)

Figure 6. Simulation results (a) 3-level DC-MLI using SPWM +PD ($V_{dc}/3$), (b) FFT for SPWM +PD
(c) 3-level DC-MLI using SPWM +POD ($V_{dc}/6$), (d) FFT for SPWM +POD
(e) 3-level DC-MLI using SVPWM ($V_{dc}/3$), (f) FFT for SVPWM




(a) (b)

Figure 7. Simulation results: CMV with (a) 3-level DC-MLI using proposed SVPWM (CMV=$V_{dc}/6$)

## 6. Implementation of Proposed SVPWM Scheme Mapping For CMV Reduction

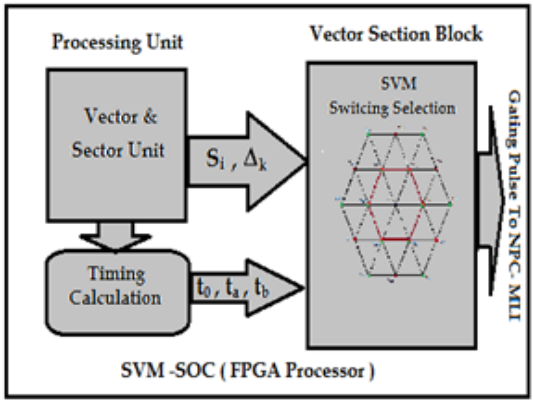
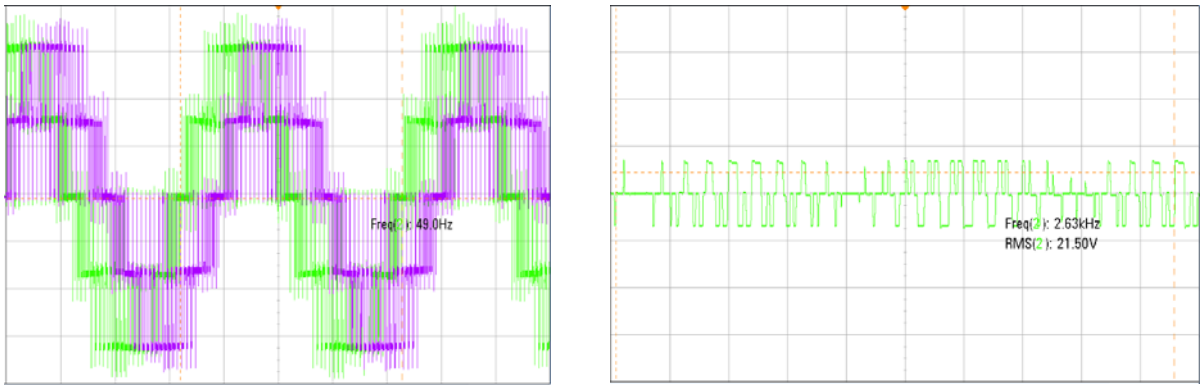



Figure 8. (a) SVPWM switching mapping SVPWM Switching table for Sector 1 - $\Delta_1$ for Partial Elimination of CMV

Table 1. SVPWM Switching table for Sector 1 - $\Delta_1$

| SECTOR | SWITCHING STATES IN CONVENTIONAL METHOD | SWITCHING STATES IN PARTIAL ELIMINATION METHOD |
|---|---|---|
| Zero vectors | [000](0)<br>[111]($V_{dc}/2$)<br>[-1-1-1](-$V_{dc}/2$) | [000](0) |
| Short vectors | [100]($V_{dc}/6$)<br>[0-1-1](-$V_{dc}/3$)<br>[110]($V_{dc}/3$)<br>[00-1](-$V_{dc}/6$) | [100]($V_{dc}/6$)<br>[00-1](-$V_{dc}/6$) |
| Medium vector | \[10-1](0) | [10-1](0) |
| Large vectors | [1-1-1](-$V_{dc}/6$)<br>[11-1]($V_{dc}/6$) | [1-1-1](-$V_{dc}/6$)<br>[11-1]($V_{dc}/6$) |

The Proposed Switching Schemes for SVPWM is mapped in using processing unit and Vector Section Block. In this processing unit based on the reference vector the sector $S_i$, sub triangle $\Delta_k$ & Timing Calculations ($t_a$,$t_b$& $t_{0)}$ of the switches are calculated. In this Vector Section block selecting the switching state for reduced CMV




(a) (b)

Figure 9. Simulation results: (a) 3-level DC-MLI Line Voltage SVPWM Proposed 100 V/div, 5 ms/div (b) reduced CMV up to ( $V_{cmv}$= 16.66V =$V_{dc}$/6) ,50 V/div, 5 ms/div

## 7. RESULT DISCUSSION

Table 2 shows Comparison of Different PWM technique with THD in Pole Voltage, Line Voltage &CMV an induction motor when connected to a 3 leveldiode clamped In comparison, the PD pole Voltage is slightly less than the Peoposed SVPWM schems and its Produce Vdc/3 CMV. The PD-SPWM technique cannot further reduce the CMV because its switching states are not controllable. The magnitude of the CMV (maximum) is reduced to Vdc/6 using the APOD-SPWM and POD-SPWM techniques. but THD value for pole Voltage and pole current is high compare to Proposed SVM. The proposed SVPWM changes with a step of Vdc/6. However, the THD in the line voltage is lower then the POD & APOD-SPWM technique. Comparisons of the THD in the pole voltage and the line voltage, and the CMV are given in Table-2. The proposed SVM not only plummeting the CMV its also Hoarding pole voltage with better harmonics spectrum. The Algorithm Implemented in same in the process without adding any hardware and loop up table

Table 2. Comparison of THD in Pole Voltage, Line Voltage &CMV

| PWM technique | THD | | CMV |
|---|---|---|---|
| | Pole Voltage | Line voltage | |
| PD [4] | 35.15% | 18.01% | $\pm V_{dc}/3$ |
| POD | 39.53% | 20.03% | $\pm V_{dc}/6$ |
| APOD[ 1 ] | 38.69% | 22.44% | $\pm V_{dc}/6$ |
| Proposed SVPWM | 20.5% | 5.3% | $\pm V_{dc}/6$ |

## 8. CONCLUSION

A conventional two-level inverter generates CMV which is responsible for a leakage current and the premature failure of motor bearings. A multilevel inverter has the inherent ability to reduce CMV. Simulation and experimental results prove that the PD-SPWM & POD-SPWM technique reduces the magnitude of CMV to $V_{dc}$/6 and that it has a minimum THD in the line voltage and current. The proposed SVPWM technique further reduces the magnitude of CMV to $V_{dc}$/6 at the cost of reducing the THD in the line voltage and current. A multilevel inverter reduces the dv/dt in its output voltage and therefore the leakage current is also reduced.

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