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Simulation and dSPACE Based Implementation of Various PWM Strategies for a New H-Type FCMLI Topology

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ABSTRACT

Depending on the number of levels in output voltage, inverters can be divided into two categories: two level inverter and Multi Level Inverters (MLIs). An inverter topology for high voltage and high power applications that seems to be gaining interest is the MLI. In high power and high voltage applications, the two level inverters have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating.In this paper, a three phase H + type FCMLI (Flying Capacitor MLI) using sinusoidal reference, third harmonic injection reference, 60 degree reference and stepped wave reference are initially developed using SIMULINK and then implemented in real time environment using dSPACE. In H-type FCMLI with R-load it is inferred that bipolar COPWM-C provides output with relatively low distortion for 60 degree reference and bipolar COPWM-C strategy is found to perform better since it provides relatively higher fundamental RMS output voltage for THI reference. The five level output voltages of the chosen MLIs obtained using the MATLAB and dSPACE based PWM (Pulse Width Modulation) strategies and the corresponding %THD (Total Harmonic Distortion), V_{RMS} (fundamental), CF (Crest Factor) and FF (Form Factor) are presented and analyzed.

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1. INTRODUCTION

Since, the multilevel converter has been introduced in the year of 1975. It converts DC-to-AC which requires many DC sources and sums them to output a time-varying wave. Multilevel converters have a lot of advantages to offer in medium- to high-voltage range of applications. The term multilevel states that power conversions are produced by utilizing multiple small voltage levels. Small voltage step makes the multilevel inverter has to withstand better voltage, fewer harmonics, lower switching losses, electromagnetic compatibility, voltage with high capability and good power quality. Multilevel converters can synthesize waveforms using more than two voltage levels. Control schemes employed in multilevel converter applications include, PWM and Line frequency control. The former allows variation of output voltage whereas the latter does not. In general, PWM control requires the use of more than one carrier waveform to cater for the various levels. This multilevel inverter produces AC output voltage in stepped wave (staircase shape) get from sinusoidal waveform.

Batschauer et al., [1] proposed a large portion of energy can be processed by the VSI by employing a single multi-pulse rectifier, while smaller power shares are processed within the half-bridge modules. Thus,

the requirements for galvanically insulated dc sources are reduced. Changliang Xia et al., [2] proposed a boost three-level chopper on the front of a three-level diode-clamped inverter is used and the switch-signal phase delay control is balancing the neutral point potential of three-phase inverter based on the characteristics of boost three-phase chopper. As the boost chopper is also used for maximum power point tracking, the controller with dual PI regulators is designed for the chopper. Davoodnezhad et al., [3] proposed a controller which achieves a line-to-line harmonic performance that is very close to open-loop phase disposition pulse width modulation, while retaining all of the dynamic benefits of hysteresis current regulation. Ewanchuk and Salmon [4] proposed a three-phase parallel inverter system can be operated using a single three-limb coupled inductor, significantly improving the system power conversion density. Ghazanfari et al., [5] proposed an inverter configuration is capable of generating low distortion, near-sinusoid stepped output voltage even with fundamental frequency switching. The total harmonic distortion (THD), switching losses, fault-tolerant feature of the proposed multilevel inverter-based power supply is compared with that of the conventional two-level inverter-based power supplies. Gupta et al., [6] proposed a generalized multiband hysteresis modulation and its characterization have been proposed for the sliding-mode control of cascaded H-bridge multilevel-inverter (CHBMLI)-controlled systems. Net hysteresis bandwidth for a given desired maximum switching frequency of the inverter is determined. Hasegawa and Agaki [7] proposed the dc mean voltages of all the four split dc capacitors can be balanced, independent of inverter control. Jin Wang and Ahamadi [8] based on equal area criteria and harmonic injection. The maximum of five switching angles show that the proposed method can be used to achieve excellent harmonic elimination performance. Ui-Min Choi et al., [9] presented a strong balancing ability at all regions and furthermore it is very simple to implement in both space vector modulation and carrier-based PWM methods. Zoubir et al., [10] suggested a new multilevel active power filter using switches meticulously controlled. Heru Pratomo et al., [11] proposed a simple strategy of controlling a balanced voltage capacitor in single phase five-level inverter.

2. H-TYPE FCMLI (Flying Capacitor Multi Level Inverter)

Meynard and Foch introduced a flying-capacitor based inverter in 1992. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The circuit topology of the H-type flying capacitor multilevel inverter is shown in Figure 1. This topology has a ladder structure of DC side capacitors where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. One advantage of the flying capacitor based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. Table 1 shows a list of all the combinations of phase voltage levels that are possible for the circuit shown in Figure 1. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels. In addition to the (m-1)/2 DC link capacitors, the m-level FCMLI will require (m-1) × (m-2)/2 auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches.

Table 1. H-type flying capacitor multilevel inverter - switches states and output voltage levels

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	V_{ao}	V_{bo}	$V_{ab}=V_{RN}$
0	0	1	1	1	1	0	0	-1/2 Vdc	1/2Vdc	-Vdc
0	0	1	1	0	1	0	1	-1/2 Vdc	0	-1/2 Vdc
0	1	0	1	1	1	0	0	0	1/2 Vdc	-1/2 Vdc
1	0	1	0	1	1	0	0	0	-1/2 Vdc	1/2 Vdc
1	1	0	0	1	1	0	0	1/2 Vdc	1/2 Vdc	0
0	0	1	1	0	0	1	1	-1/2 Vdc	-1/2 Vdc	0
0	1	0	1	0	0	1	1	0	-1/2 Vdc	-1/2 Vdc
1	1	0	0	0	1	0	1	1/2 Vdc	0	1/2 Vdc
1	0	1	0	0	0	1	1	0	-1/2 Vdc	1/2 Vdc
1	1	0	0	0	0	1	1	1/2 Vdc	-1/2 Vdc	Vdc

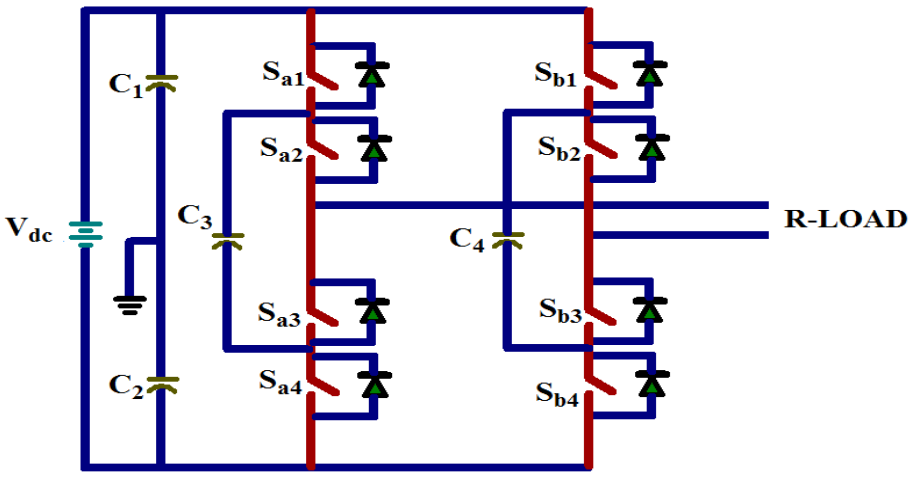

Figure 1. Single phase H-type flying capacitor multilevel inverter

3. SIMULATION RESULTS AND ANALYSIS

The simulated output voltage is shown for only one sample value of m_a=0.8. The following parameter values are used for simulation: V_{dc} = 440V, R(load) = 100 ohms, $C_1 = C_2 = C_3$ and C_4 = 1000 e-3 Farad, f_c =2000 Hz and f_m = 50 Hz. Figure 2 shows the sample five level output voltage generated by PDPWM strategy with sine reference and its FFT plot is shown in Figure 3. Tables 2 to 5 show the comparison of %THD, V_{RMS} (fundamental), CF and FF for different PWM strategies with various references.

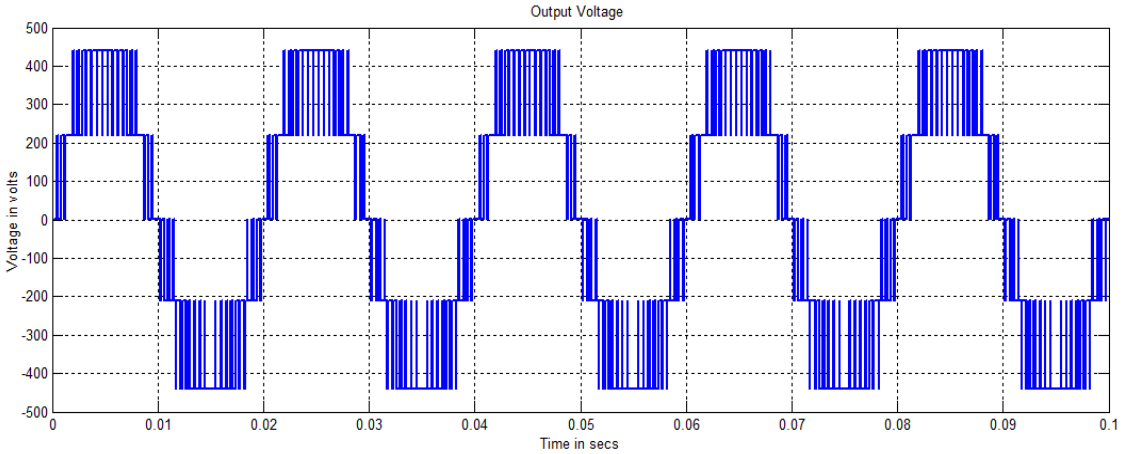

Figure 2. Sample output voltage generated by PDPWM strategy for H-type FCMLI with sine reference

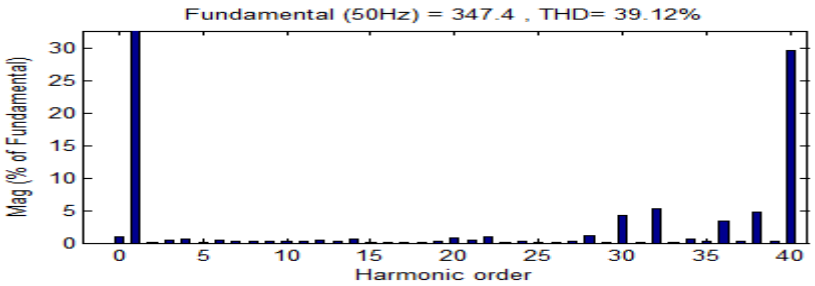

Figure 3. FFT plot for output voltage generated by PDPWM strategy for H-type FCMLI with sine reference

Table 2. % THD of output voltage (R-phase) of H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference								Third harmonic injection reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	27.38	27.30	27.96	32.29	31.59	26.02	27.53	27.4	28.92	28.67	29.0	31.12	32.34	30.81	29.0	28.9
0.9	34.20	34.10	34.67	38.81	36.50	29.97	33.38	34.0	36.31	35.78	36.08	36.17	37.27	34.84	36.1	36.3
0.8	39.12	38.88	39.36	45.59	41.48	33.94	39.01	39.0	41.89	41.73	42.21	41.71	41.16	38.01	41.9	42.0
0.7	42.85	42.66	43.01	55.42	47.33	37.14	42.17	43.2	44.93	44.85	45.28	51.14	44.56	40.70	45.1	44.9
0.6	44.98	45.03	45.01	66.62	55.71	40.67	44.88	45.0	43.70	43.24	43.66	60.39	51.17	43.38	43.7	43.7
m_a	60 degree PWM reference								Stepped wave reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	22.57	22.21	22.61	26.75	27.98	23.56	22.55	22.6	24.67	25.54	24.66	29.65	31.53	25.47	25.0	24.6
0.9	31.69	31.47	32.09	33.33	34.41	29.59	31.93	31.7	33.76	33.71	33.32	38.81	36.02	29.82	33.2	33.80
0.8	38.26	38.11	38.38	38.47	38.70	33.13	38.86	38.3	39.68	39.12	39.29	46.81	40.01	31.88	39.4	39.9
0.7	42.66	42.38	42.69	47.17	42.91	36.16	42.69	42.6	42.41	42.03	42.77	56.28	47.72	37.16	42.9	42.6
0.6	43.46	43.18	43.78	58.71	46.94	39.31	42.66	43.2	46.88	47.56	46.92	68.12	54.42	40.49	45.5	47.1

Table 3. V_{RMS} (fundamental) of output voltage (R-phase) of H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference								Third harmonic injection reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	308.9	308.8	308.4	315.8	331.7	332.3	309.1	308	359	359	359.4	363.5	369.4	369.8	358	358.8
0.9	277.4	277.3	276.9	288.2	310.4	311.2	277.7	277	322.6	322.7	323	335.5	345.2	345.6	323	322.5
0.8	245.6	246	245.5	258	286.6	287.8	245	245	285.6	286.3	286.2	305.2	322.1	323.2	285	285.8
0.7	213.6	213.3	213.6	221.1	259.8	260.5	214.4	213	249	249	249.1	264.8	297.4	298.9	249	249.4
0.6	182	181.6	182	182.5	231.1	233	180.5	182	212	211.7	211.8	219.1	267.5	268.5	211	212.2
m_a	60 degree PWM reference								Stepped wave reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	363.5	363.3	1652.2	365.5	372.2	356.7	363.4	363	313.6	309.1	307.9	318.8	333.6	332.3	312	313.6
0.9	326.2	326.6	881.3	336.4	345.1	331	326.9	326	280.5	278.5	276.9	288.8	307.4	306	279	280.3
0.8	289	288.9	506.8	306.3	321.7	308.8	290.1	289	248.6	250.4	247.8	259.7	287.5	285.5	249	248.1
0.7	251.8	251.6	310.4	267.8	296.7	283.8	251.9	251	218.1	221.8	218.4	226	260.3	260.5	218	217.5
0.6	214.6	214.7	193.2	222.1	271.1	257	214.3	214	185.7	188.1	186	186.5	233.8	235.4	186	185.1

Table 4. CF of output voltage (R-phase) of H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference								Third harmonic injection reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	1.414	1.414	1.414	1.413	1.413	1.414	1.414	1.41	1.414	1.414	1.414	1.414	1.414	1.414	1.414	1.414
0.9	1.414	1.414	1.414	1.414	1.413	1.4142	1.4141	1.41	1.4141	1.414	1.414	1.414	1.4142	1.4140	1.414	1.4142
0.8	1.414	1.414	1.414	1.413	1.414	1.4141	1.4142	1.41	1.4142	1.414	1.414	1.414	1.4141	1.4142	1.4143	1.4142
0.7	1.414	1.414	1.414	1.414	1.414	1.4142	1.4141	1.41	1.4144	1.414	1.414	1.414	1.4142	1.4142	1.139	1.4141
0.6	1.414	1.414	1.414	1.413	1.414	1.4141	1.4144	1.41	1.4141	1.414	1.414	1.414	1.4138	1.4141	1.4145	1.4142
m_a	60 degree PWM reference								Stepped wave reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	1.414	1.4142	1.4140	1.4142	1.4142	1.4140	1.4144	1.414	1.4142	1.4141	1.4140	1.4140	1.4142	1.4142	1.4144	1.4142
0.9	1.414	1.4139	1.4142	1.4140	1.4143	1.4141	1.4141	1.413	1.4139	1.4143	1.4145	1.4141	1.4141	1.4143	1.4140	1.4141
0.8	1.414	1.4143	1.4143	1.4139	1.4143	1.4145	1.4139	1.414	1.4139	1.4141	1.4144	1.4143	1.4142	1.4143	1.4146	1.4139
0.7	1.414	1.4145	1.4143	1.4141	1.4142	1.4143	1.4140	1.414	1.4140	1.4143	1.4143	1.4141	1.4141	1.4142	1.4145	1.4142
0.6	1.414	1.4145	1.4139	1.4142	1.4142	1.4143	1.4143	1.414	1.4141	1.4141	1.4145	1.4144	1.4140	1.4141	1.4142	1.4143

Table 5. FF of output voltage (R-phase) of H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference								Third harmonic injection reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	792.0	701.8	685.3	45.90	1184.6	INF	INF	404.6	INF	1631	1562.6	98.50	2462.6	INF	35810	2990
0.9	533.4	462.1	453.9	30.49	862.22	INF	27770	533.4	2304	827.	807.5	59.91	1380.8	INF	INF	1007.
0.8	279.8	311.3	21.7	21.16	636.88	INF	24500	351	446.2	485.	477	38.05	894.7	INF	28500	408.2
0.7	284.8	213.3	211.48	12.77	463.92	INF	21440	239.4	503.1	383.	289.6	19.27	619.5	INF	24980	300.4
0.6	176.6	146.4	146.77	7.753	355.53	INF	18050	152	322.3	177	177.98	9.78	453.3	INF	21180	228.1
m_a	60 degree PWM reference								Stepped wave reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	INF	1730	1652.2	100.1	2658.5	INF	INF	2796.1	15680	657	699.7	48.30	1235.5	INF	10400	627.3
0.9	858.4	882.7	881.3	60.61	1380.4	INF	1634.5	881.3	475.4	464	477.4	32.93	768.5	INF	27990	2548.1
0.8	672.0	515.8	506.8	39.52	919.1	INF	INF	444.7	147.1	329	427.2	22.46	598.9	INF	24960	322.2
0.7	387.3	310.6	310.4	21.89	659.3	INF	8396.6	426.9	84.53	233	240	13.90	456.6	INF	21880	148.97
0.6	206.3	193.4	193.2	10.83	475.6	INF	INF	206.3	70.87	160	163.1	8.68	354.2	INF	6220	107.61

4. dSPACE BASED IMPLEMENTATION

The required offline simulations of gate signal generation blocks/models for the chosen five level inverter using various PWM strategies are initially carried out using SIMULINK. The models developed in SIMULINK are then compiled, downloaded and executed in real time on dSPACE system. Since dSPACE system can be easily interfaced with SIMULINK, a 'build' function in SIMULINK automatically converts any SIMULINK model into a targeted C code using the real time workshop of dSPACE system. The C code becomes source for the real time interface of dSPACE system, which with the help of a C compiler/linker, produces and downloads the machine code in the dSPACE board. Finally to read or write the internal variables of the control system, dSPACE control desk provides a user friendly GUI environment that enables the user to observe vital data in the system. The external voltage in the range -10V to +10V are converted into quantized values in the range -1V to +1V for ADC and vice versa for the DAC unit of dSPACE system. Hence gains of 0.1 and 10 are included to compensate for this signal conversion. The generated switching pulses are taken from the DAC or input/output ports of dSPACE system and fed to pulse amplifiers before being applied to the gates of MOSFETs of the prototypes of the chosen inverters.

5. HARDWARE RESULTS

This section presents the results of experimental work carried out on chosen H-type FCMLI using dSPACE DS1103 controller board. The results of the experimental study are shown in the form of the oscillograms of PWM outputs of chosen MLI and corresponding harmonic spectra. Experiments are performed with appropriate m_f (same as in simulation studies) and for different values of m_a. The corresponding V_{RMS} (fundamental) of output voltages and their % THD and CF values are calculated (from the FFT spectrum obtained), tabulated and analyzed. The experimental output voltages and the corresponding harmonic spectra are shown for only one sample value of m_a=0.8. Figure 4 show the entire hardware setup for H-type FCMLI. Figure 5 to 8 shows the sample experimental output voltage of chosen MLI obtained using dSPACE/RTI with triangular carrier PDPWM strategy and sine, THI, 60 degree and stepped wave reference. Tables 6 – 8 show the comparison of %THD, V_{RMS} (fundamental) and CF for different PWM strategies with various references. Figures 9 to 11 display the control desk settings, built function settings and variations of modulating signals.

The following parameter values are used for experimentation: V_{dc}=30V in view of laboratory limitations, R(load)=100Ω, f_c=2000Hz and f_m=50Hz, m_f=40.

Figure 4. Entire hardware setup for H-type FCMLI

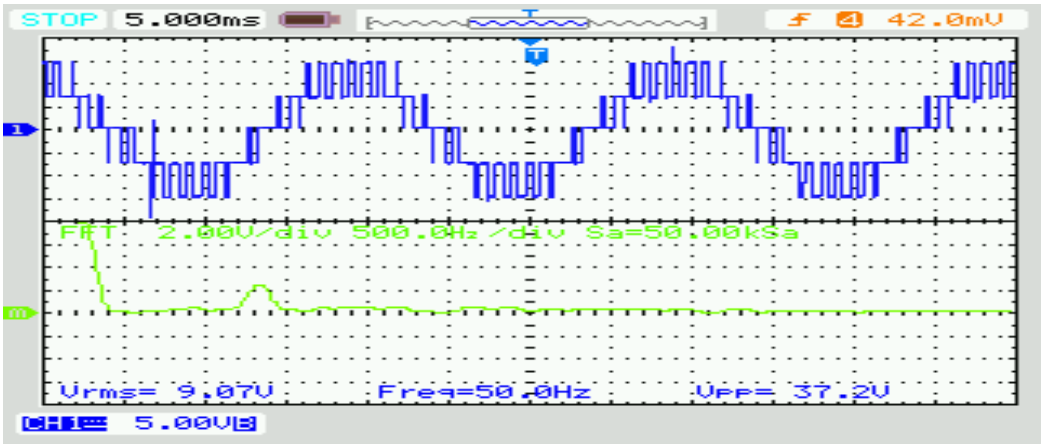

Figure 5. Sample output voltage of H-type FCMLI with PDPWM strategy (m_a=0.8, sine ref.)

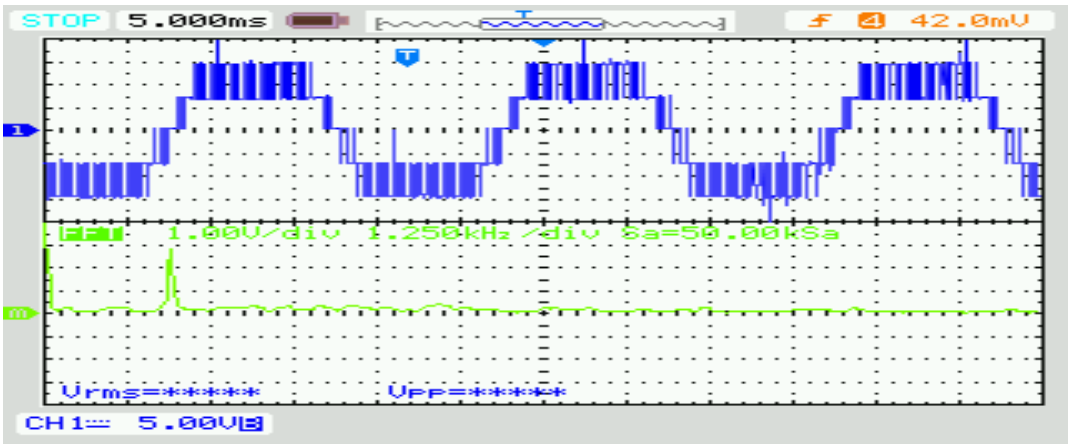

Figure 6. Sample output voltage of H-type FCMLI with PDPWM strategy (m_a=0.8, THI ref.)

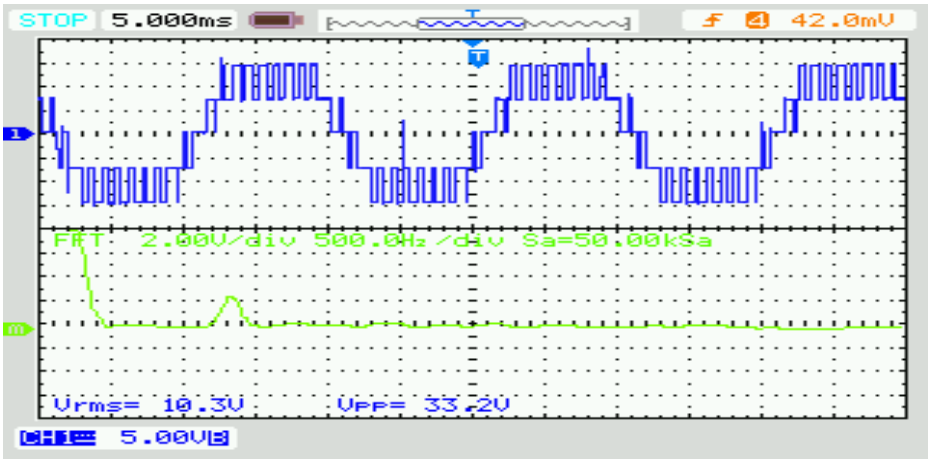

Figure 7. Sample output voltage of H-type FCMLI with PDPWM strategy (m_a=0.8, 60 degree ref.)

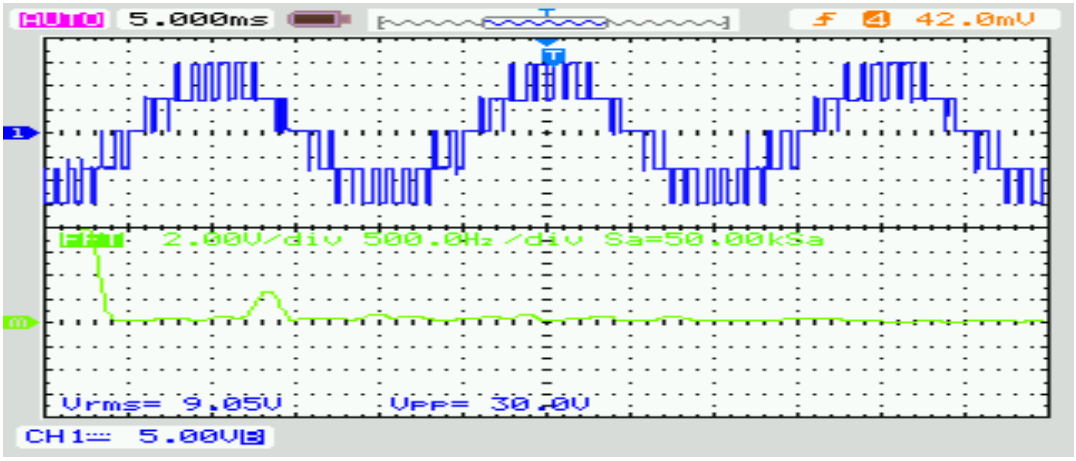

Figure 8. Sample output voltage of H-type FCMLI with PDPWM strategy (m_a=0.8, stepped wave ref.)

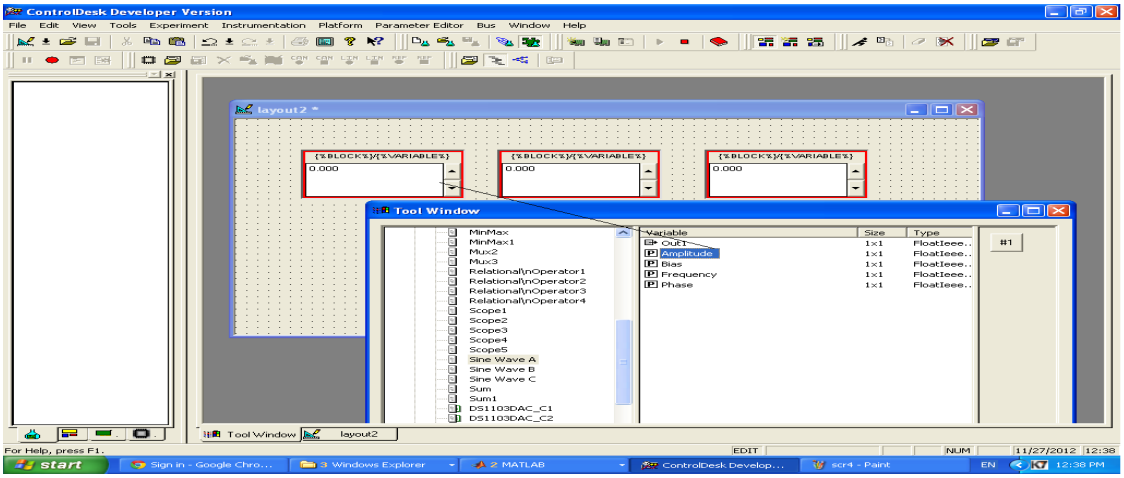

Figure 9. dSAPCE screen to set the amplitude of the modulating signal

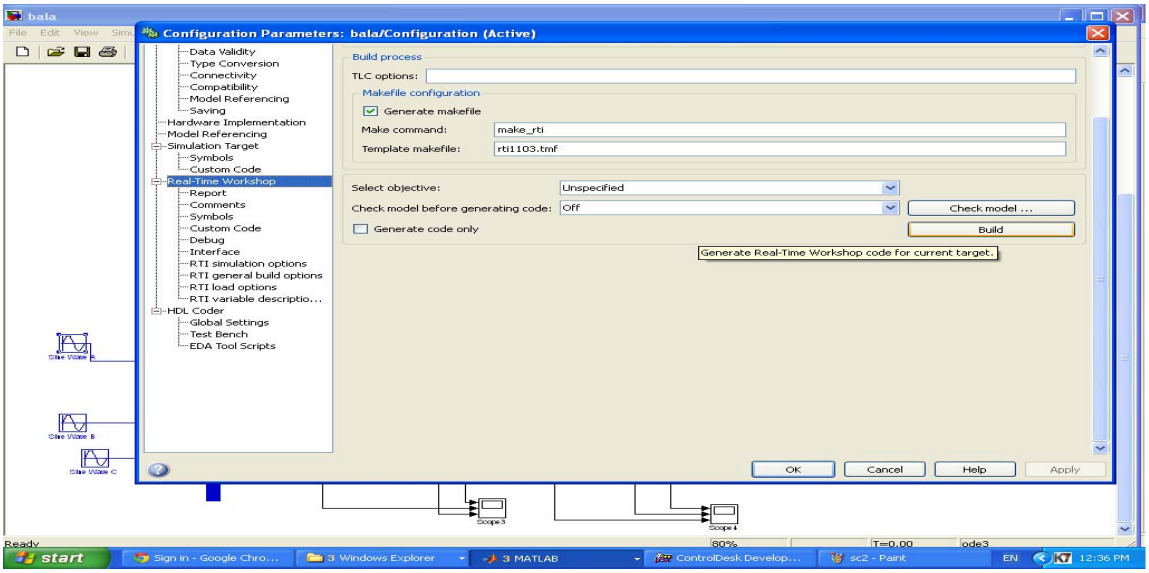

Figure 10. dSAPCE screen to set the built function

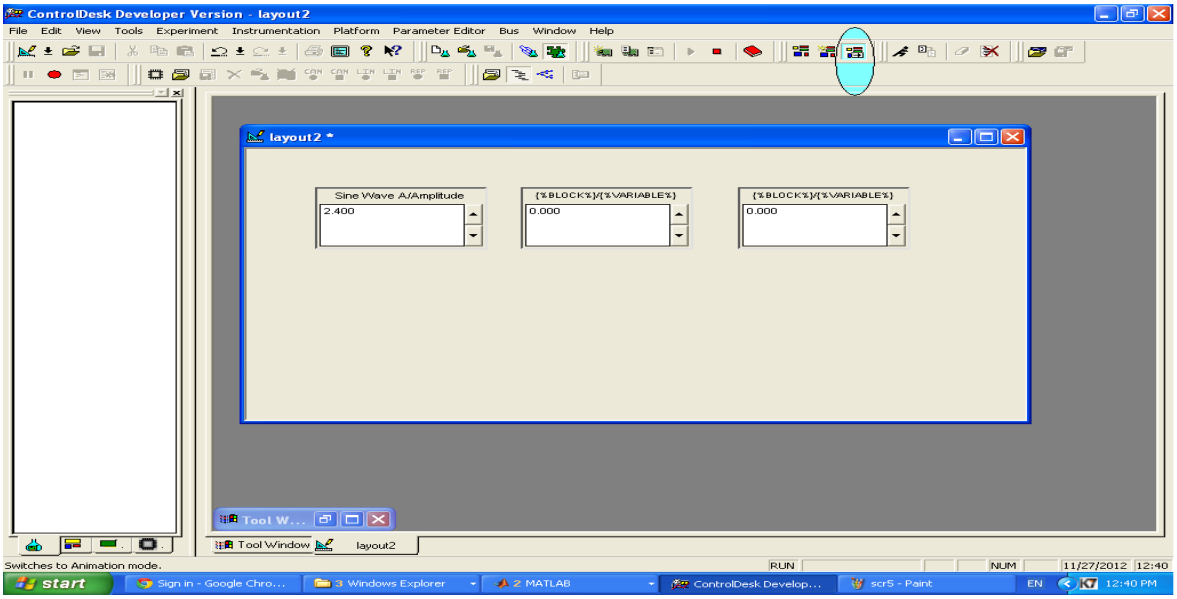

Figure 11. dSAPCE screen with control desk option

Table 6. % THD of output voltage (R-phase) of H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference								Third harmonic injection reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	21.79	16.58	22.91	30.41	20.61	20.61	7.07	7.07	18.02	13.22	11.99	16.58	8.66	13.22	11.2	8.66
0.9	23.45	22.36	22.36	33.16	27.38	28.28	8.66	9.01	22.27	15.55	14.73	18.2	13.22	29.15	12.4	13.22
0.8	26.62	23.97	23.45	33.54	30.16	34.64	11.45	10.3	25.23	17.02	17.32	19.36	15.81	38.40	14.1	15.81
0.7	29.15	24.67	28.1	37.74	31.62	39.83	13.22	11.1	26.92	19.97	20.0	21.21	31.51	49.43	18.4	21.79
0.6	30.41	30.0	30.0	46.57	34.17	47.95	35.36	15.0	30.26	20.68	20.5	26.45	33.06	51.42	24.1	27.45
m_a	60 degree PWM reference								Stepped wave reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	13.22	10.0	7.90	27.18	18.02	18.70	12.24	16.5	25.0	19.36	22.91	25.0	25.49	29.15	8.66	7.70
0.9	19.36	11.18	8.66	30.17	23.97	23.16	13.46	19.9	28.24	22.91	22.36	34.27	27.83	33.6	14.1	8.66
0.8	20.61	20.0	15.81	36.22	29.58	27.49	14.14	28.2	29.5	27.38	27.83	35.0	30.0	36.79	15.0	10.0
0.7	24.49	27.83	18.02	47.63	32.97	39.61	18.6	28.7	36.40	28.28	29.1	44.65	32.5	37.08	19.3	13.22
0.6	30.2	30.14	21.21	48.67	41.25	46.36	24.3	35.6	39.6	30.38	30.82	46.09	35.70	43.08	26.2	15.81

Table 7. V_{RMS} (fundamental) of output voltage (R-phase) of H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference								Third harmonic injection reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	10.7	10.8	10.6	11.3	11.4	10.8	10.5	10.6	12.2	12.1	12.0	12.7	12.4	12.7	11.5	12.2
0.9	9.87	9.84	9.67	11.1	11.0	9.76	9.45	9.75	11.21	11.1	11.2	12.0	11.9	11.6	10.4	11.23
0.8	9.07	8.77	8.56	10.5	10.6	8.95	8.82	8.82	10.52	10.5	10.2	11.4	11.5	10.2	9.82	10.4
0.7	8.0	8.32	8.06	9.78	9.78	8.09	8.01	7.92	9.56	9.39	9.18	10.3	10.2	9.5	9.01	9.37
0.6	6.97	7.10	7.11	9.04	8.97	7.17	7.11	7.16	8.45	8.49	8.23	9.23	9.45	9.1	8.11	8.7
m_a	60 degree PWM reference								Stepped wave reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	12.4	12.2	12.3	12.4	12.9	12.5	12.2	12.4	10.8	10.7	10.9	11.8	11.5	10.8	10.7	10.9
0.9	11.4	11.4	11.3	12.3	12.2	11.3	10.4	11.4	9.50	9.79	10.2	11.2	11.2	9.87	9.31	10.8
0.8	10.3	10.3	10.3	10.8	11.5	10.6	10.1	10.3	9.05	8.90	9.02	10.5	10.8	8.90	9.27	9.87
0.7	9.28	9.23	9.15	10.7	10.8	9.85	9.68	9.14	8.28	8.00	8.20	9.90	10.0	8.42	8.77	9.08
0.6	7.91	7.81	7.84	10.2	10.0	8.56	8.97	8.03	7.08	7.02	7.02	9.11	9.18	7.13	7.78	7.90

Table 8. CF of output voltage (R-phase) of H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference								Third harmonic injection reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	1.420	1.379	1.603	1.353	1.5	1.555	1.619	1.443	1.377	1.404	1.491	1.283	1.395	1.425	1.573	1.48
0.9	1.671	1.504	1.530	1.567	1.472	1.772	1.798	1.507	1.311	1.684	1.464	1.416	1.453	1.560	1.732	1.59
0.8	2.050	1.870	1.880	1.476	1.471	1.810	1.927	1.689	1.416	1.542	1.529	1.561	1.504	1.774	1.843	1.82
0.7	1.875	1.899	1.836	1.758	1.738	1.953	2.122	1.931	1.600	1.810	1.873	1.519	1.696	1.905	2.008	1.93
0.6	2.266	2.183	2.095	1.847	1.694	2.078	2.390	2.067	1.751	1.802	1.834	1.641	1.830	1.989	2.231	2.08
m_a	60 degree PWM reference								Stepped wave reference							
	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF	PD	POD	APOD	CO-A	CO-B	CO-C	PS	VF
1	1.225	1.229	1.227	1.266	1.310	1.224	1.385	1.395	1.388	1.383	1.477	1.271	1.530	1.611	1.691	1.70
0.9	1.385	1.429	1.318	1.292	1.254	1.353	1.673	1.421	1.578	1.705	1.539	1.589	1.553	1.722	1.718	1.40
0.8	1.611	1.524	1.699	1.555	1.504	1.443	1.831	1.436	1.657	1.719	1.718	1.514	1.462	2.101	1.682	1.50
0.7	1.799	1.744	1.715	1.523	1.453	1.705	1.735	1.652	1.799	1.875	2.256	1.494	1.61	1.912	1.812	1.83
0.6	2.212	1.907	2.334	1.647	1.53	1.775	1.694	2.129	2.090	2.435	2.378	1.964	1.764	2.089	2.275	2.02

6. CONCLUSIONS

Based on the research on hybrid multilevel inverter topology, this work presented a general multilevel hybrid topology. According to the controllable freedoms given in this general hybrid topology, several new hybrid topologies may be constructed, which enriches the multilevel inverter topology collection. In H-type FCMLI with R-load it is inferred that bipolar COPWM-C provides output with relatively low distortion for 60 degree reference and bipolar COPWM-C strategy is found to perform better since it provides relatively higher fundamental RMS output voltage for THI reference. The hybrid topology is simulated using MATLAB - SIMULINK and then implemented in real time using dSPACE. The results are satisfactory.

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