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A Shunt Active Power Filter for 12 Pulse Converter Using Source Current Detection Approach

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ABSTRACT

A shunt Active Power Filter (APF) with current detection at the source side is considered as a closed-loop system from the view of the whole power distribution system, which is expected with better harmonics filtering performance compared with conventional current detection methods such as load current detection and open loop control. This paper introduces an efficient source current detection method (direct) control scheme to mitigate the grid current harmonics generated by the twelve pulse converter. The proposed system uses Control Rectifier (12 –pulse converter) which efficiently regulates the DC voltage by varying the angle of each 6 pulse converter. Moreover, the proposed system uses three winding transformer which eliminates the harmonics during equal angles switching at each six pulse converter which in turn simplifies the operation of the SAPF. The proposed system is simulated in MATLAB SIMULINK to evaluate the performance of the proposed system.

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1. INTRODUCTION

The Solid-State power electronic converters are generally used for providing controlled power to electrical loads like personal computers; printers; heating, ventilation, and air conditioning (HVAC) systems; adjustable speed drives, elevator drive, arc furnaces and arc welders. These loads are considered as nonlinear loads because of the fact that they pull harmonic currents from the ac mains along with their active power demand. In addition, with unbalanced condition of three-phase systems, they draw neutral currents in excess. The injected harmonics, reactive power demand, imbalance, and large neutral currents pose more load on the utility power system equipment, raise the power system losses, and thus degrade the power system efficiency.

Compensation techniques like passive or active power filtering (APF) are helpful in improving the line side power quality for the purpose of complying with harmonic guideline standards like IEEE 519-1992 [1]. Power quality issues can be resolved with passive filters, although, passive filters have their own demerits; which comprise of the source impedances dependency, parallel/series resonance, aging of passive components, unmanageable filter currents and reactive power that could be generated [2]. Owing to semiconductor device development, the APF tends to become a highly hopeful compensator solution [3]–[6].

Based on the installation techniques, the APF could be classified as a series APF, a hybrid APF, and a shunt APF. The series APF is always connected in series to the grid bay transformer. Along with voltage protection for loads, it could also yield good harmonics current filtering with a variety of control techniques [7]–[9]. Nonetheless, the availability of a series-connected transformer hugely increases the complexity involved with design and deployment in practical applications, which reduce the use of the series APF. The hybrid APF is introduced with the thought of its economic feasibility to merge the use of an APF and a PF. By this, the capacity requirement of the APF could be reduced to a dramatic level [10]–[13]. But, for most normal voltage level condition and normal capacity requirement, the hybrid APF is still too complex to be taken into consideration. In this situation, the shunt APF is yet the most extensively employed kind to handle harmonics currents. It is directly connected in shunt between the grid source and loads, without any modification to the networks already present, which is easier for installation or cut off in the practical field.

Also, the aim of the shunt APF system is to be able to balance the harmonics current from the load side, thus ensuring that there is no distortion in the current in the source side.

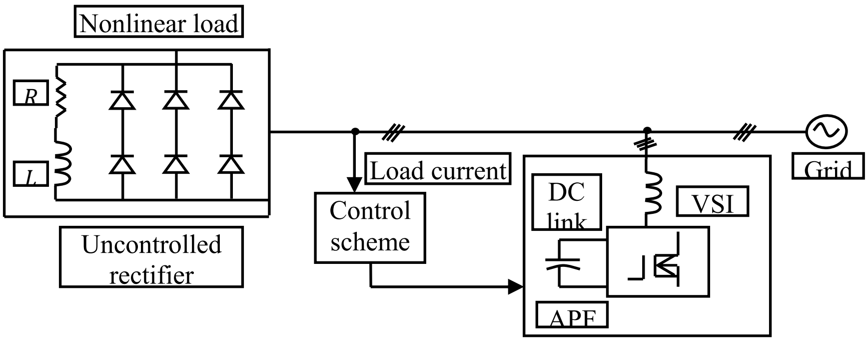


Figure 1. The Basic Shunt Active Power Filter Architecture

Figure 1 illustrates the basic Shunt active power filter architecture consisting of grid, VSI, APF and load current detection based control scheme. This conventional system makes use of the three phase diode bridge rectifier design regarded as non linear load producing unregulated output. But in case, if the industry needs a regulated output for any of the applications, this conventional system design may not be a suitable option. In addition, if the output of the uncontrolled rectifier is greater than 800 V, this system is not again appropriate. Thus, controlled rectifier will be a desired choice for handling the above mentioned scenarios.

Controlled rectifiers are usually employed in high power applications, particularly at medium voltage (MV) levels because of higher reliability, robustness, lower complexity, and lesser power losses. In addition to the variable power factor, the chief disadvantage is the harmonics produces results in a power quality issue at the converter ac-side [12], [14], [15].

The basic control scheme of the shunt APF could be the load current detection kind. Hence, from the purview of the whole power distribution system and with respect to the source current being the control target, the control scheme with load current detection is always treated as an open loop system, with the control target being indirectly controlled, as shown in Figure 1. The important objective of this paper is the introduction of an efficient closed loop controlling scheme for the purpose of eliminating the grid current harmonics produced by the twelve pulse converter.

2. PROPOSED 12 –PULSE CONVERTER FOR REGULATES DC VOLTAGE BY VARYING THE ANGLES

The proposed system architecture is illustrated in figure 2. It chiefly consists of 12 pulse converter made of controlled rectifier, three phase three winding transformer, active power filter and the associated control scheme. The proposed system is built with a three-winding transformer (star/tapped star/delta) and one SAPF connected to secondary taps which provides filter side voltage reduction, without the need for a high bandwidth step down transformer. This auto—transformer type configuration limits the voltage rating of the SAPF switches, thereby, increasing the switching frequency limit. This arrangement helps in mitigating the net amp-turns within the transformer window area for the current harmonic components that is generated by each 6-pulse converter, along with the net harmonics balanced by the SAPF.

In order to be able to control the SAPF, a source detection control scheme has been brought into use in this work which is explained clearly in the sections below.

Importance of Control Rectifier in the Proposed System

The three phase fully controlled bridge converter has been probably the most extensively used power electronic converter to be employed in the medium to high power applications. Three phase circuits are preferred in the case of large power being involved. The controlled rectifier can offer controllable output dc voltage in a single unit in place of three phase autotransformer and a diode bridge rectifier. The controlled rectifier is got by substituting the diodes of the uncontrolled rectifier with thyristors. Control over the output dc voltage is got by applying a control on the conduction interval of each thyristor. This method is referred to as phase control and converters are also known as "phase controlled converters".

Significance of twelve pulse converter and three winding transformer

In this presented architecture, twelve pulse converter and the three winding transformer play a significant role in the overall performance of the system. For instance, twelve-pulse configuration comprises of two sets of converters connected in series as illustrated in Figure 2.

The resultant ac current is obtained by the sum of the two Fourier series of the star connection (equation 1) and delta connection transformers (equation 2):

$$\mathrm{i_A} = \frac{2\sqrt{3}}{\pi}\mathrm{I_D}\left(\cos\omega\,\mathrm{t} - \frac{1}{5}\cos 5\omega\mathrm{t} + \frac{1}{7}\cos 7\omega\mathrm{t} - \frac{1}{11}\cos 11\omega\mathrm{t} + \cdots.\right) \quad (1)$$

$$\mathrm{i_A} = \frac{2\sqrt{3}}{\pi}\mathrm{I_D}\left(\cos\omega\,\mathrm{t} + \frac{1}{5}\cos 5\omega\mathrm{t} - \frac{1}{7}\cos 7\omega\mathrm{t} - \frac{1}{11}\cos 11\omega\mathrm{t} + \cdots.\right) \quad (2)$$

$$\mathrm{i_A} = 2\left(\frac{2\sqrt{3}}{\pi}\right)\mathrm{I_D}\left(\cos\omega\,\mathrm{t} - \frac{1}{11}\cos 11\omega\mathrm{t} + \frac{1}{13}\cos 13\omega\mathrm{t} - \frac{1}{23}\cos 23\omega\mathrm{t} + \ldots.\right) \quad (3)$$

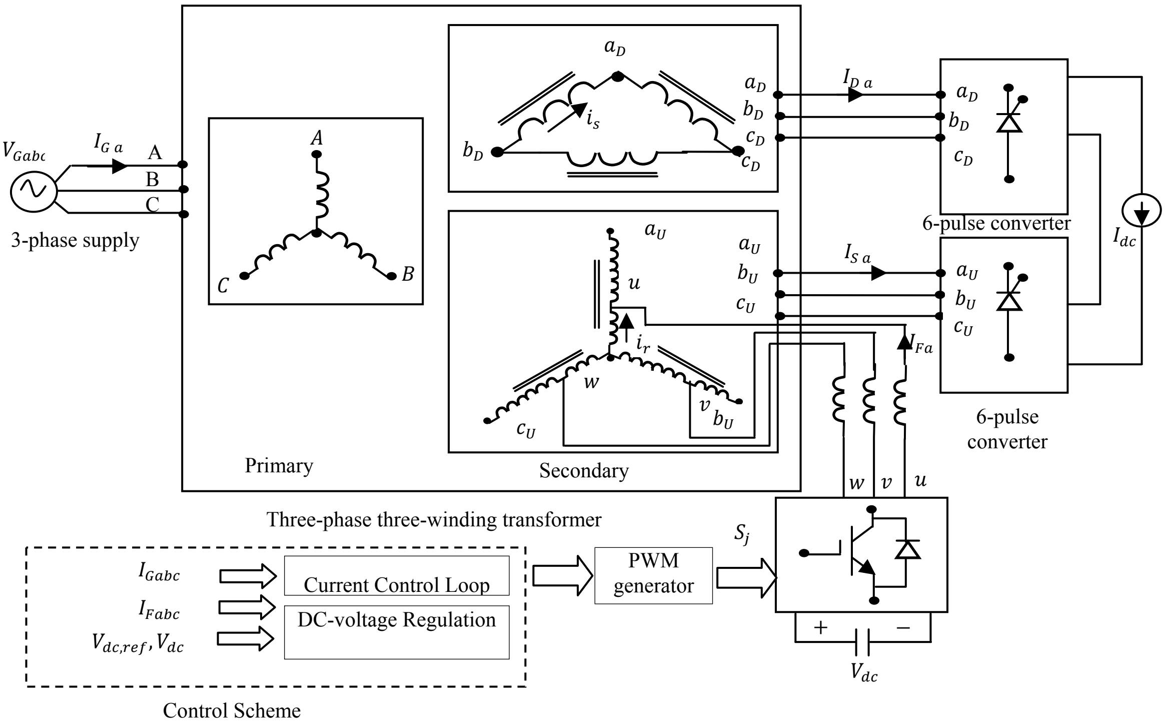


Figure 2. The proposed source current detection based SAPF Architecture

The series only has the harmonics of order $12k \pm 1$. The harmonic currents of orders $6k \pm 1$ (With k odd), i.e. 5th, 7th, 17th, 19th, etc., circulates between the two converter transformers but does not enters the ac network. The resulting line current for the twelve-pulse rectifier is as shown in Figure 3, which is similar to a sinusoidal waveform than earlier line currents. The instantaneous dc voltage also becomes smoother with this connection. The twelve-pulse was got with a 30° phase-shift between the two secondary transformers.

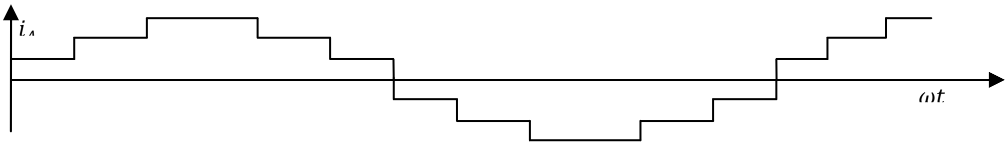


Figure 3. The result line current for the twelve-pulse rectifier

2.1. Controlling Scheme of the Proposed System

The intention of this work is focusing on the controlling scheme to be able to control the active power filter. The important objective is compensating the grid current. The significant operation of the controlling scheme is the elimination of the disturbances or harmonics in the grid current that is generated by the non linear load (twelve pulse converter) by means of injecting of current from APF. This way, this injection of current has to be in a controlled manner through efficient control scheme. The section below provides a discussion about the two conventional controlling methods and influenced by those conventional controlling techniques, an effective controlling scheme is proposed which is capable of overcoming the limitations of the conventional controlling techniques.

2.1.1. Conventional Controlling Schemes

This section offers to discuss about the conventional controlling techniques that are regarded as the influence for the proposed controlling scheme.

1. Load current detection method
2. Open loop control method

2.1.1.1. Load Current Detection Method

The control loop architecture of the conventional Load current detection method is illustrated in Figure 4. The generation of compensating signal by the load current detection method involves three control stages, which are; reference extraction, current control, and the PWM [3], [6], [11]–[13].

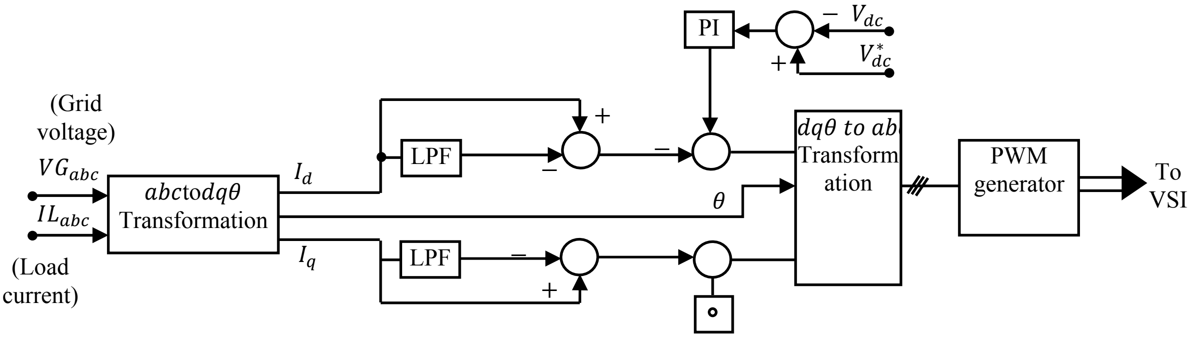


Figure 4. The control loop architecture of the conventional Load current detection method

Where id and iq are instantaneous active and reactive currents respectively, (V_{dc}) And (V_{dc}^*) denotes the change in dc link voltage and reference dc link voltage respectively, $id1h +$ and $iq1h +$ refers to the first harmonic active current of positive sequence and harmonic reactive current of positive sequence.

Owing to the feedback of load current, the delay that is produced in the reference signals and/or the original injected current delays have an effect on the APF compensation quality, particularly at times when the switching frequency is low. These kinds of controlling techniques are known as indirect methods. As a result, the compensated mains current THD can be greater than the standards allowed. Few solutions have been presented for solving a problem of this kind. Many traditional APF techniques made use of low-pass filters (LPF) for extraction of the current harmonics and classical controllers for the current control like PI or hysteresis [14]. This results in harmonic mis-cancellation because of phase shifts and reference tracking errors which in turn deteriorate filtering performance.

2.1.1.2. Open Loop Control Method

The fundamental compensation principle of the open-loop controlled shunt SAPF for a nonlinear load is illustrated in Figure 5. By understanding the nonlinear load operating conditions, the firing delay angle, and the load current which is supposed to be ripple free, the nth harmonic current that has to be injected at the PCC can be computed. This current cancels the respective nth harmonic supply current. These favorable compensating harmonic current vectors can be decided by fixing the correct magnitudes and phase-shift angles of the harmonic contents. A Phase Locked Loop (PLL) is employed for the purpose of synchronizing the compensation process. The dc-link capacitor voltage is controlled to obtain a power balance between the filter and the mains by means of a separate control loop. It is controlled at a level just for avoiding over modulation after the addition of the harmonic modulating signals.

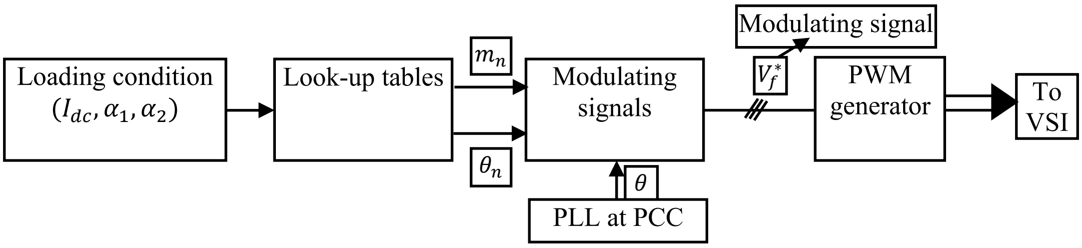


Figure 5. The fundamental compensation principle of the open-loop controlled shunt SAPF

With an aim to generalize the algorithm and accomplish current harmonic compensation on the basis of the knowledge of I_{dc}, α_1, and$\alpha_2$under every possible loading conditions; tables of harmonic modulating signal information are built, off-line. Two kinds of harmonic tables are needed: tables for the amplitude m_n and tables for the phase angles θ_n. These tables are utilized as look-up tables in which their data is interpolated for generating any necessary values of $m_n$and θ_n, which removes the selected harmonic orders as illustrated in Figure 5. To achieve the required output voltage from the 12 pulse converter, the firing delay angle of each six pulse converter has to be varied in a continuous manner. However, this offline controlling scheme is not propoer for the dynamic firing delay angle variation of the 12 pulse converter. The above mentioned factor deteriorates the overall performance of the APF in the dynamic varying condition.

2.2. Proposed Source Current Detection Method

On the basis of the investigation of the aforementioned controlling schemes, the source current detection scheme has been presented. The proposed scheme provides the benefits of both the traditional load current detection and open loop control schemes and, at the same time, eliminates their limitations. The proposed control scheme is simpler in structure and does not need a harmonics extraction algorithm. The proposed control scheme is derived based on the employment of the vector resonant (VR) controller, and it is got through a series of transformations that are applied to the conventional load current detection scheme is shown in figure 6.

The control scheme chiefly comprises of three parts: phase-locked loop (PLL), dc link voltage regulation, and current control loop. The PLL link is helpful for tracking the real-time phase information of grid voltage VGabc for online adjustment of the resonant frequency of resonant controllers; dc-voltage regulation is applied for maintaining the dc voltage; and the current control loop forms the core part to implement harmonics filtering.

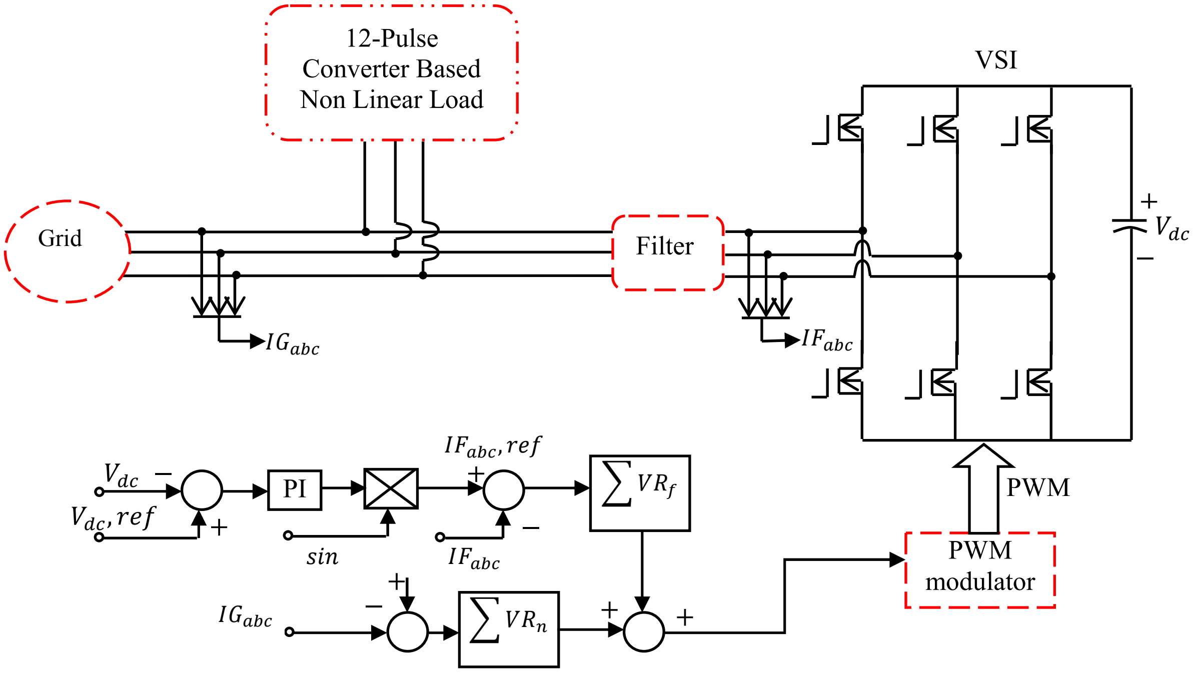


Figure 6. The proposed control scheme using the employment of the vector resonant (VR) controller

Also, the gain effect of pulse width modulation controlled VSI K_{pwm} is indicated as unity for the purpose of simplifying the analysis, with its influence in the controller taken into consideration. The line inductor is the system control plant, and it could be realized as

$$P(s) = \frac{1}{sL_{ac} + R_{ac}} \tag{4}$$

Where L_{ac} and R_{ac} are the equivalent inductance and resistance ofL, respectively.

The current controller is necessary for the current control loop, and the VR controller is used for each control scheme that is discussed in this paper. The VR controller keeps all the advantages of the resonant controller, like efficiency in computation and zero steady-state errors for the regulation of the ac signal. Also, in comparison with the PR controller, the VR controller has an amazing feature of selectivity. As shown in [19], the expression for VR controller could be given as

$$VR(s) = k_{VR} \frac{s(s + \frac{R_{ac}}{L_{ac}})}{s^2 + (n\omega_e)^2} \tag{5}$$

Where k_{VR} is the gain of the controller, and $n\omega_e$ is the corresponding resonant frequency.

In addition to this, the VR controller the control plant takes into account, and its good selectivity renders it quite apt for the selective APF, with which the restricted device capacity could be reasonably placed for compensating the most harmful harmonics, and the potential resonance in power distribution networks could be avoided with flexibility. Selective harmonics compensation could be realized by the implementation of cascade VR controllers.

VR_n in the current control loop. Subscript n denotes the selected harmonics order. As shown in Figure 3, VR_n is the superposition of each VR controller, with every controller tuned on one harmonics order. In this condition, the reference tracking ability of the current control loop in Figure 3 could be defined as

$$\frac{i(s)}{i_{ref}(s)} = \frac{P(s).\sum VR_n(s)}{1 + P(s).\sum VR_n(s)} \approx \sum \frac{P(s).VR_n(s)}{1 + P(s).VR_n(s)} \tag{6}$$

3. RESULTS AND DISCUSSIONS

The performance of the proposed source current detection based SAPF for a 12-Pulse Converter is simulated in MATLAB/Simulink environment using the Sim Power-System toolbox. The result is evaluated based on the steady state and the dynamic performance of the proposed system and the achieved sinusoidal current with minimal THD obtained at the grid.

Parameters such as grid voltage (VGabc), grid current (IGabc), Star connected secondary output current (ISabc), Delta connected secondary output current (IDabc), Filter current (IFabc) of the proposed system are evaluated to demonstrate its proper functioning. Moreover, Total Harmonic Distortion (THD) of grid current is analyzed for determining the power quality at grid side.

3.1. 12 – Pulse Converter Results Validation of Proposed System

The result obtained shows the significance of the 12-pulse converter used in the proposed system. It is clearly observed from the results that, for equal firing delay angles of each 6-pulse converter, for example (A_1=α_2=30°) as shown in Figure 7 and (A_1=α_2=0°) as shown in Figure 8. The achieved grid current IGabc waveforms without compensation for both scenarios are near sinusoidal with minimum THD. The THD obtained for the firing delay angles (A_1=α_2=30°) and (A_1=α_2=0°) is 10.89% and 6.07% respectively. This is due to fact that, 12-pulse converter reduces the harmonic orders such as 5th, 7th, 17th, 19th, etc. Hence, only limited injection by the SAPF is enough to maintain the optimal output.

A1=a2=30

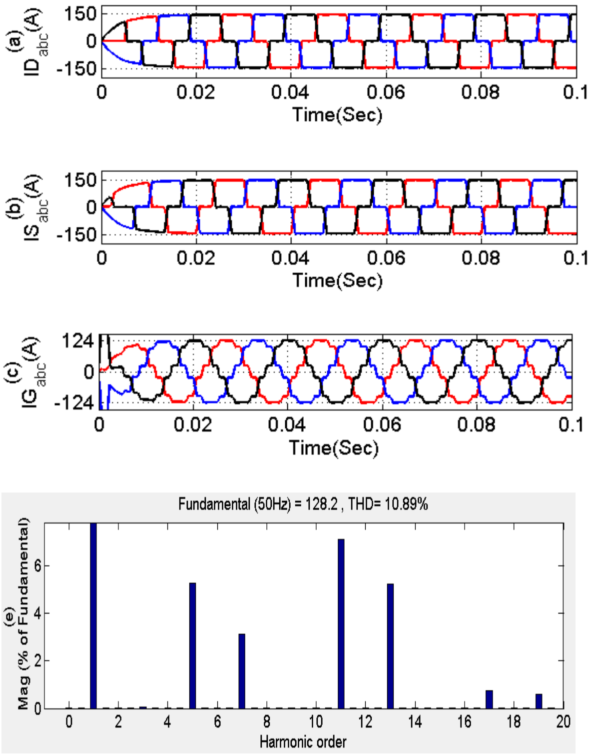


Figure 7. The result for equal firing delay angle $A_1 = \alpha_2 = 30°$ of 12-pulse converter

A1=a2= 0

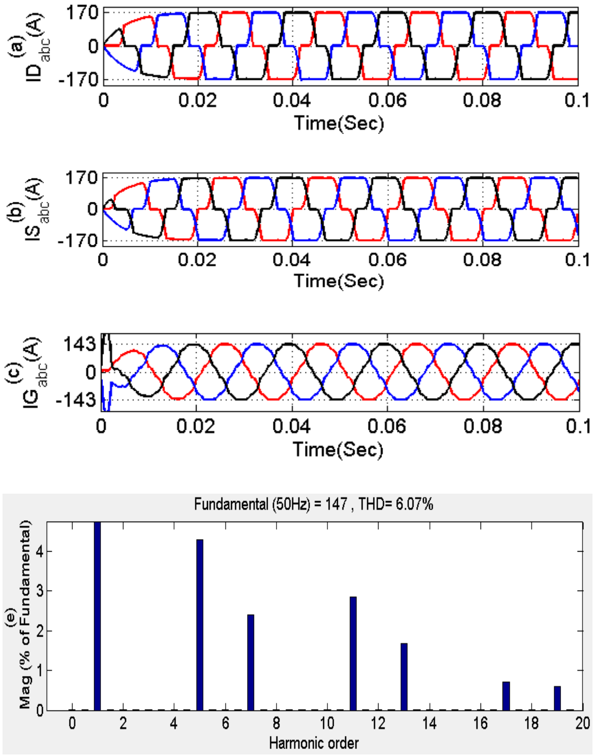


Figure 8. The result for equal firing delay angle $A_1 = \alpha_2 = 0°$ of 12-pulse converter

3.2. Different Firing Delay Angles

The experimental results obtained for each 6-pulse converter with different firing delay angles without compensation, for example (A_1=53°; α_2=10°) and (A_1=10°; α_2=53°) as shown in Figure 9 and 10 respectively. Respective Star connected secondary output current waveform (ISabc) and delta connected secondary output current waveforms (IDabc) and moreover, grid voltage VGabc is shown for both the scenarios in Figure 9(d) and Figure 10 (d). It is clearly observed from the results that, for varied firing delay angles, the obtained THD without compensation is high. For instance, the THD obtained with firing delay angle of (α_1=53°; α_2=10°) and (α_1=10°; α_2=53°) is 23.28% and 20.75% respectively. This increase in THD is because of the impact of the harmonic orders such as 5th, 7th, 11th, 13th, 17th, 19th etc.

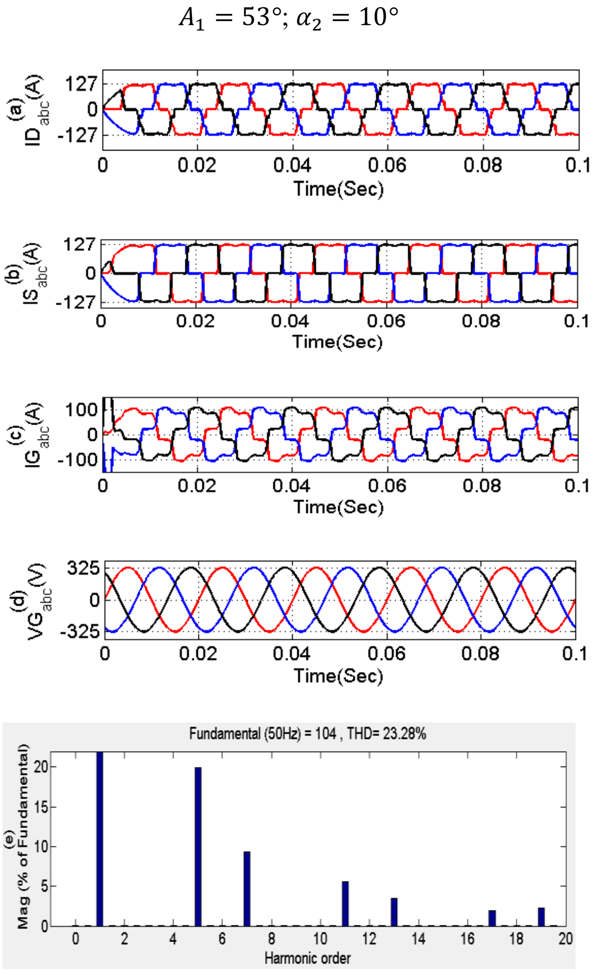


Figure 9. The result for different firing delay angles $A_1 = 53°; \alpha_2 = 10°$ without compensationof 12-pulse converter

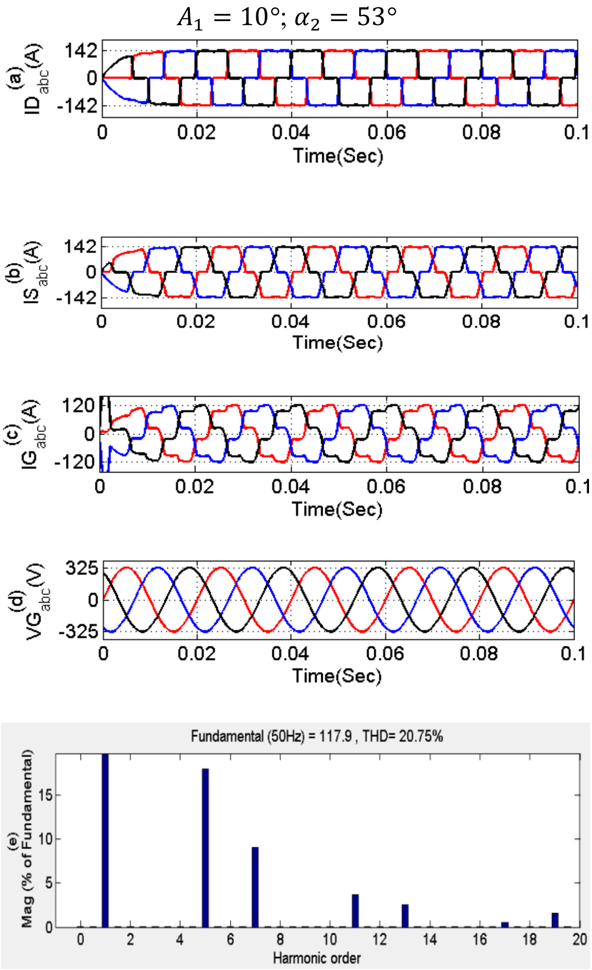
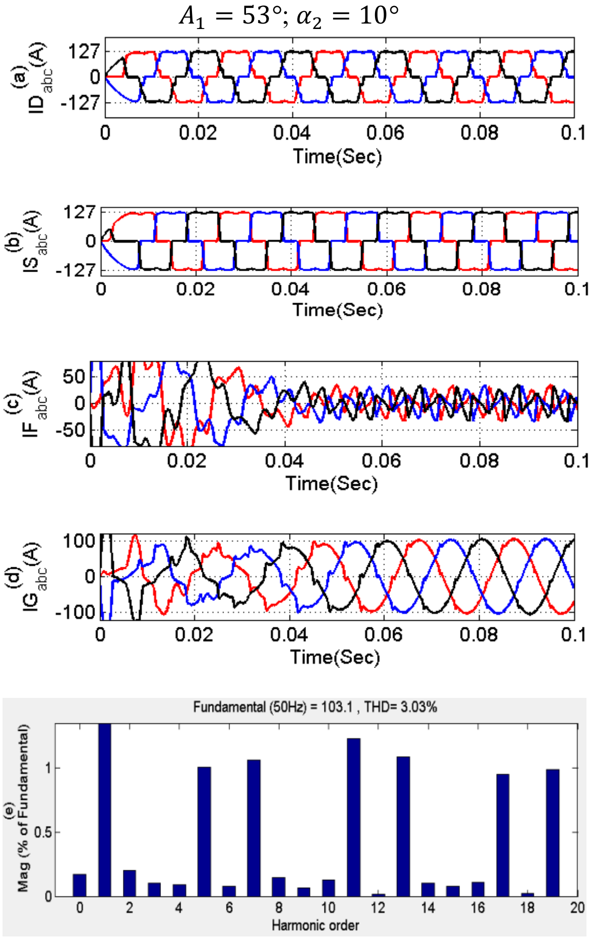


Figure 10. The result for different firing delay angles $A_1 = 10°; \alpha_2 = 53°$ without compensationof 12-pulse converter

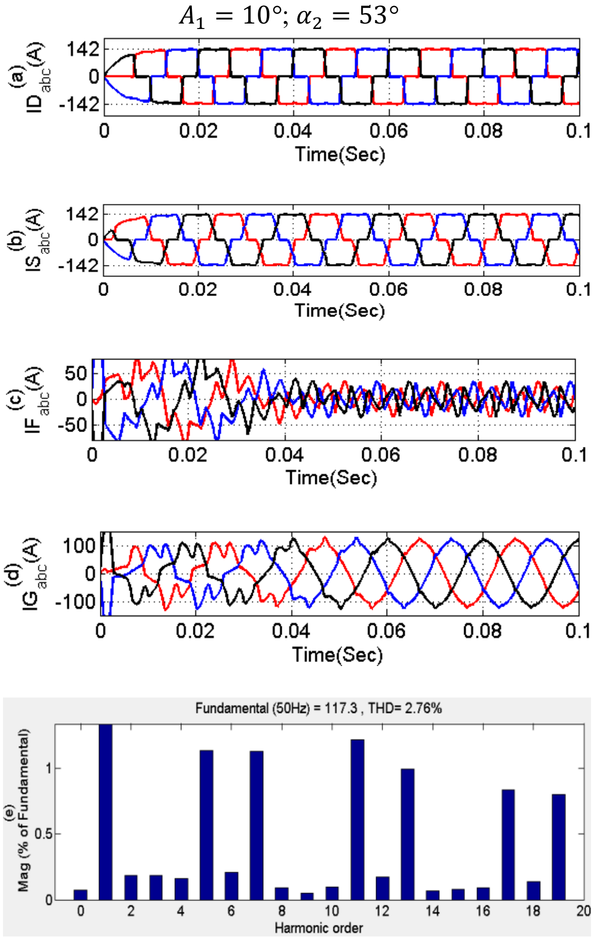
3.3. Evaluation of After Compensation

The experimental results for each 6-pulse converter with different firing delay angles after compensation, for (A_1=53°; α_2=10°) and (A_1=10°; α_2=53°) as shown in Figure 11 and 12 respectively. Due to the varied firing delay angles, the obtained THD without compensation is high. Thus, compensation is required. The results show the injected waveform (IFabc) for harmonic minimization. For instance, the THD obtained after compensation with firing delay angle of (α_1=53°; α_2=10°) and (α_1=10°; α_2=53°) is 3.03% and 2.76% respectively. This minimization in THD is achieved mainly due to injected current IFabc which compensates the harmonic orders such as 5th, 7th, 11th, 13th, 17th, 19th etc.



$A_1 = 53°; \alpha_2 = 10°$

Figure 11. The result for different firing delay angles $A_1 = 53°; \alpha_2 = 10°$ after compensationof 12-pulse converter



$A_1 = 10°; \alpha_2 = 53°$

Figure 12. The result for different firing delay angles $A_1 = 10°; \alpha_2 = 53°$ after compensationof 12-pulse converter

4. CONCLUSION

This paper proposed an efficient source current detection based SAPF for a 12-Pulse Converter. The result is evaluated based on the steady state and the dynamic performance of the proposed system. The performance of the system has been evaluated based on the angles (α_1 and α_2) of the twelve pulse converters. Three scenarios namely (α_1= α_2), (α_1≠ α_2), and sudden change in switching angles have been evaluated in the simulation and the corresponding results are obtained. It is observed from the results that during equal angle scenario, better THD is obtained based on the phase shifting of the three phase three winding transformer used in the proposed system. However, during different angle condition at the 12 pulse converter, the THD generated at the grid side has been minimized using proposed SAPF. The dynamic performance of the proposed system has also been analysed by sudden variation of the 12 pulse converter angle in which the timing response of the proposed system is observed to be significant. Thus, the proposed system clearly satisfies the IEEE 519-1992 power quality standard.

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