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A Simple Strategy of Controlling a Balanced Voltage Capacitor in Single Phase Five-Level Inverter

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ABSTRACT

The five-level inverter has been used for many applications in renewable energy systems. Even though its harmonic distortion was lower than the conventional two-level inverter. The five-level converter has some disadvantages such as increasing power semiconductor, complex pulse width modulation control methods, and problem with the voltage balancing of the capacitor. This paper aims to propose a modified five-level inverter based on sinusoidal pulse width modulation using phase shifted carrier to enhancing the capacitor voltage balancing. This modified five-level inverter reduces the overall cost and the complexity of the pulse width modulator. Thus making the proposed control system highly simple. The performance and its controller were validated by means of standard laboratory equipments. The analysis, simulation and implementation result showed better performance of five-level inverter.

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1. INTRODUCTION

Multilevel inverters have recently been developed to obtain good power quality. The general concept of this inverter is to use the power semiconductor switches to perform the conversion power. When compared to conventional power conversion approaches, there are some advantages such as a higher power production waveform quality and the reduced the voltage stress on load, high-voltage capability, and low electromagnetic compatibility. Multilevel voltage source inverters have been broadly classified into three main groups [1]: The diode-clamped multilevel inverter or the multi point-clamped converter [2], the flying-capacitor multilevel converter or multi cell inverter [3], [4] and the cascade multilevel inverter separated DC source or cascaded H-bridge multilevel inverter [5]. Other multilevel inverter topologies, such as the modular multilevel inverter employing half bridge [6], and hybrid combinations of three basic groups, have also been proposed in the literature since the last years [7]-[9]

The disadvantage of multilevel power conversion is in terms of the higher number of semiconductor switches. Another disadvantage is that the small voltage steps are typically produced by isolating voltage sources or a series of capacitor. The isolated voltage sources using a series of capacitors are required for voltage balancing [2], [4], [7-9]. For certain conditions, the voltage balancing is possible to be overcome by using a redundant switch state. For a complete solution to the problems of voltage-balancing, another multilevel inverter might, however, be required [3].

Some applications for these new multilevel inverters include flexible AC transmission systems and high power medium-voltage motor drives [10], [11]. One area where multilevel inverters are particularly

suitable is that of renewable energy such as Photovoltaic, wind turbine in which efficiency and power quality are of great concerns of researchers [12], [13].

The authors in their article [14], the source voltage is not efficient in generating output voltage level. The topology, for instance can only produce five levels of output with four DC sources, while the conventional multilevel inverter can produce up to nine levels with the same amount of the same power supply. The new five-level inverter using six power semiconductor switches, two diodes and two capacitors is performed to acquire five-levels, but with a very complicated use of control system [15]. This system can be eliminated by changing the control model into an operating model based upon sinusoidal pulse width modulation using phase shifted carrier signal. This modulation technique enables the equilibrium voltage on the capacitor to always be properly maintained without any needs of sensor and complex control system. The performance of proposed topology and its controller were validated with laboratory experiments.

2. RESEARCH METHOD

In conventional multilevel inverters, power semiconductor switches are used to generate high-frequency waveform in positive and negative polarity. However, the utilization of all the switches is not required to produce the level of bipolar as practiced. This idea has been practiced by the new topology.

This topology is a hybrid multilevel topology, which separates the output voltage into two parts. The first part is called as level generation at positive polarity, requiring high-frequency switches to generate three levels. The polarity generation is another part as, the low-frequency part operating at line frequency. This topology refers to a combination of two parts. To generate a complete multilevel output, the positive levels are generated by the high-frequency part and this part subsequently is fed to an H-bridge inverter which will generate the required polarity of the output [15].

Figure 1 depicts the five-level inverter topology, the principal idea of which as a multilevel inverter is that the left stage in Figure 1 generates the three output levels and the right circuit decides about the polarity of the output voltage.

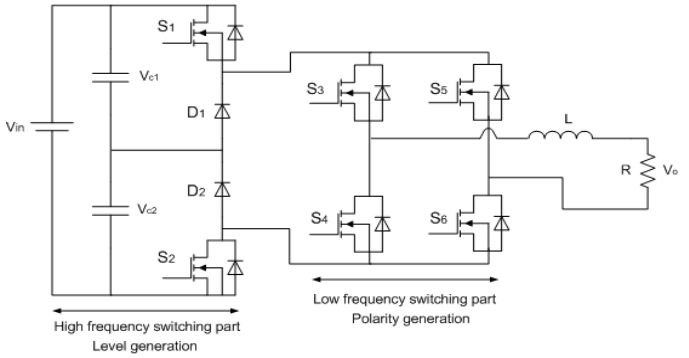


Figure 1. The multilevel inverter topology in five levels

The five-level inverter has two cycles and always ongoing work fluctuating in positive and negative values. Here is a five-level inverter working principle. The positive half cycle occurs in the current flow as shown in Figure 2 (a-d).

1. The mode of operation 1: maximum positive output (+V_{in}): S_1, S_3 is ON, connecting the load positive terminal to V_{in}, and S_6, S_2 is ON, connecting the load negative terminal to ground. All of other controlled switches are OFF; the voltage applied to the load terminals is V_{in}. Figure 2 (a) shows the current paths that are active at this stage. Mode operation 1 has an equation as follows:

$$V_i = V_L + V_o,$$
$$L\Delta i = (V_i - V_o)\, t_{on} \quad (1)$$

2. The mode of operation 2 and 3: A half positive output (+½ V_{in}): S_1, S_3 is ON, connecting the load positive terminal, and S_4, D_2 is ON, connecting the load negative terminal to ground through the C_2 (V_{C2} = ½ V_{in}). All of other controlled switches are OFF; the voltage applied to the load terminals is ½ V_{in} or D_1, S_3 is ON, connecting the load positive terminal, and S_6, S_2 is ON, connecting the load negative

terminal to ground. All of other controlled switches are OFF; the voltage applied to the load terminals is ½ V_{in}. Figure 2(b) and 2(c) show the current paths that are active at this stage. Mode operation 2 and 3 have an equation as follows:

$$V_o = L\frac{di}{dt} + \left[V_i - V_{c1}\right], \quad L\Delta i = \left[V_o - \frac{1}{2}V_i\right]t_{off} \tag{2}$$

Mode operation 3 has an equation:

$$V_o = L\frac{di}{dt} + \left[V_i - V_{c2}\right], \quad L\Delta i = \left[V_o - \frac{1}{2}V_i\right]t_{on} \tag{3}$$

3. The mode of operation 4 and 5: Zero output: This level can be generated by two switching combinations; switches D_1, D_2, S_3 and S_6 are ON, or D_1, D_2, S_4 and S_5 are ON, and all of other controlled switches are OFF; terminal output is a short circuit, and the voltage applied to the load terminals is zero. Figure 2(d) and Figure 2(e) show the current paths that are active at this stage. Mode operation 4 and 5 have an equation as follows:

$$V_o = L\frac{di}{dt}, \quad L\Delta i = \left[V_o\right]t_{off} \tag{4}$$

4. The mode of operation 6, 7, 8 and 9 are a half negative output.

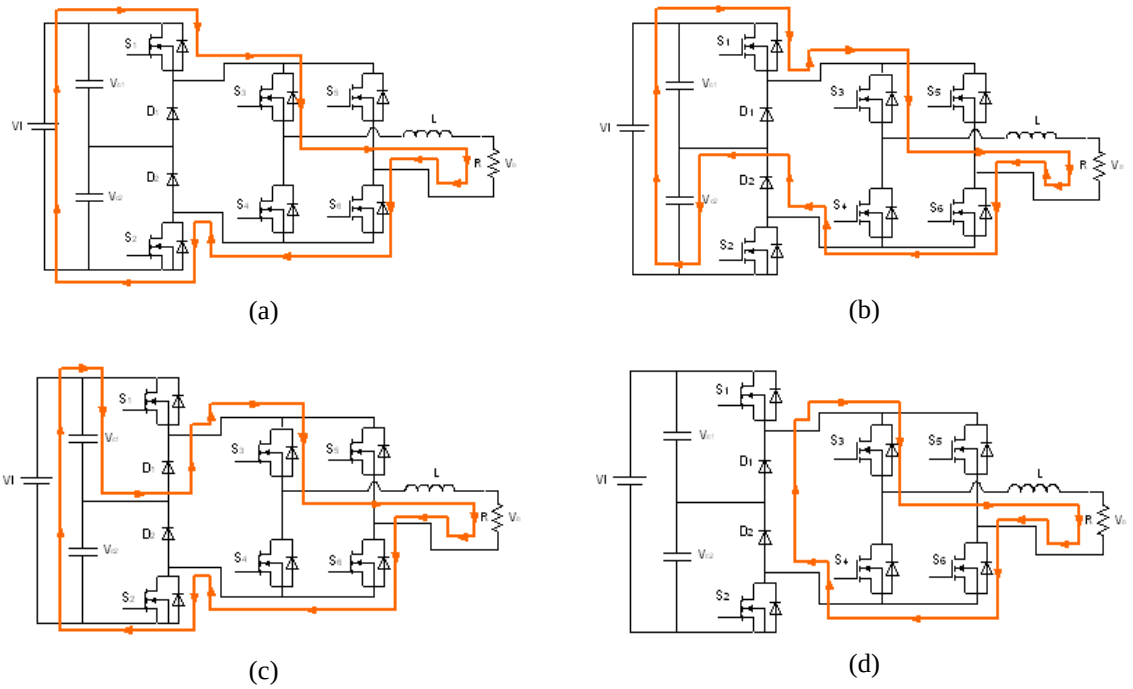


Figure 2. The mode of operation: (a) $V_o = V_{in}$ (b) V_o = ½ V_{in} (c) V_o = ½ V_{in} (d) $V_o = 0$

Thus, matrix equation obtained in the area of operations $\frac{1}{2} \leq D_1 \leq 1$ can be presented as follows,

$$\begin{bmatrix} V_o \\ V_o \end{bmatrix} = D_1 \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_i \\ \frac{1}{2}V_i \end{bmatrix}. \quad (5)$$

And the area of operations, $0 \leq D_2 \leq \frac{1}{2}$ comes to be,

$$\begin{bmatrix} V_o \\ V_o \end{bmatrix} = D_2 \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{1}{2}V_i \\ 0 \end{bmatrix}. \quad (6)$$

Thus the overall matrix equations can be presented as follows,

$$\begin{bmatrix} V_o \\ V_o \\ V_o \\ V_o \end{bmatrix} = \begin{bmatrix} D_1 \\ D_2 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_i \\ \frac{1}{2}V_i \\ \frac{1}{2}V_i \\ 0 \end{bmatrix}. \quad (7)$$

Where:

$\begin{bmatrix} D_1 \\ D_2 \end{bmatrix} = D$, $D = \frac{V_c}{V_{\text{inf}}}$, D: the modulation index.

V_c : The amplitude of the carrier signal.

V_{inf} : The amplitude of the signal information.

From the mode of operation that occurs, an equation output current ripple can be derived. An inverter output signal can be considered as a DC signal that fluctuates in the positive and negative value if the carrier frequency is very high. If the switching period is expressed as:

$$T = \frac{1}{f} = t_{on} + t_{off}. \quad (8)$$

The operation mode 1 and 2, equation output current ripple will work at the first level to the second level as presented below:

$$\Delta i = \frac{V_i^2 - 3 V_i V_o + 2 V_o^2}{(3 V_i - 4 V_o) L f}. \quad (9)$$

The equation of the output current ripple (9) is valid at the interval time, $1 \leq D_1 \leq \frac{1}{2}$. The operation mode 3 and 4, equation output current ripple will work at the second level to the third level as presented as follows:

$$\Delta i = \frac{\left(\frac{1}{2}V_i - V_o\right)V_o}{\frac{1}{2}V_i L f}. \quad (10)$$

The equation of the output current ripple (10) is valid at the interval time, $\frac{1}{2} \leq D_2 \leq 0$. At the time of negative fluctuations, the value on the other hand becomes negative.

Where:

Δi : Output current ripple

f : Switching frequency

L : Inductance of the inductor

A five-level inverter requires two capacitors as the linked series. Both capacitors are then connected to a DC voltage source. Because the capacitor voltage must be in balance, this equilibrium is determined by the charging and discharging through the power switches. Thus the amount of energy stored in the capacitor will be equal to the amount of energy stored in the inductor. The value of the capacitor can be determined as follows:

$$W_C = W_L ,$$
$$C = \frac{L \Delta I^2}{\Delta V^2} . \quad (11)$$

From the mode operation in Figure 2, two cycles can occur in operating modes including positive and negative cycles. In this way, an inverter output voltage ($+V_i$,$+½ V_i$, 0, $- ½V_i$, $-V_i$). Based on the operating mode, charging and discharge occurred in the capacitor, thus creating an automatic balance of the capacitor voltage.

A simple pulse width modulation technique to make the balance voltage on capacitor was introduced to generate the switching signals based upon Table 1. The reference signals (V_{ref}) were compared with a carrier signal ($V_{carrier}$). Figure 3 shows the resulting switching pattern. Switches S_1, and S_2 would be switching at the rate of the carrier signal frequency, whereas S_3, S_6 and S_4, S_5 would operate at a frequency that was equivalent to the fundamental frequency. The proposed scheme of a multilevel inverter topology in five levels is shown in Figure 4.

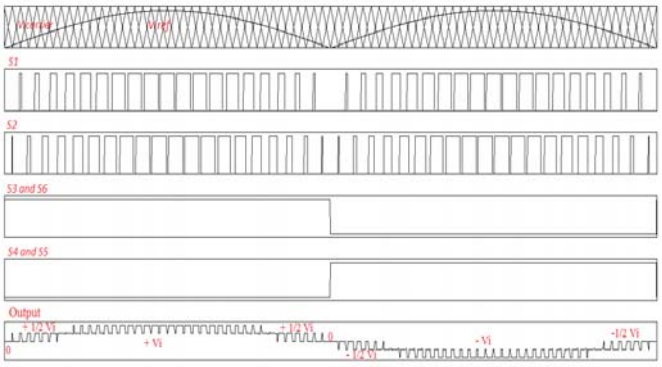


Figure 3. Switching pattern for the single-phase five-level inverter

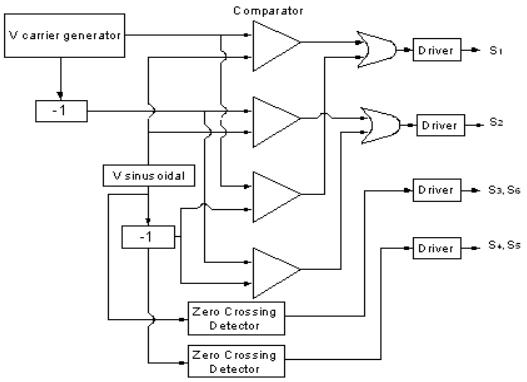


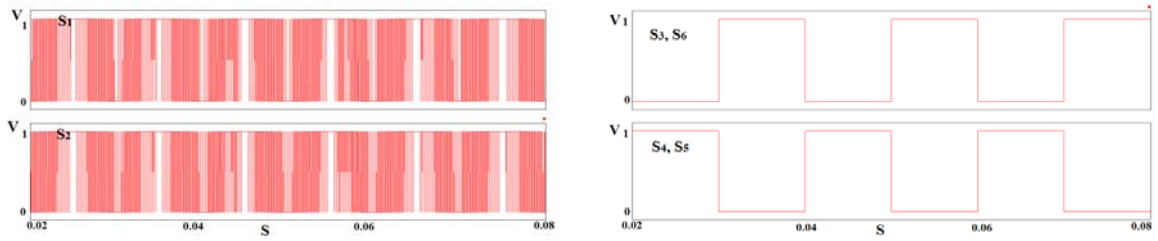
Figure 4. The proposed scheme

3. RESULTS AND ANALYSIS

Verification of the analysis and simulation that have been conducted was performed, through laboratory testing. Table 2 presents the parameters used in the simulation and implementation. This scheme (Figure 4) was implemented with ATMEGA 8535 micro-controller using data lookup tables. Meanwhile, the simulation of the control circuit as shown in Figure 4 was implemented with a Power Simulator Software. The simulation results showed a number of switching functions on each semiconductor switch device. Computational simulation resulted in the form of a switching function later in the program and inserted into a memory included in the micro-controller 8535 (Figure 5(a) and 5(b)). Figure 6(a) and 6(b) show the implementation result pulse width modulation switching signals for switches S_1–S_6 in micro-controller.

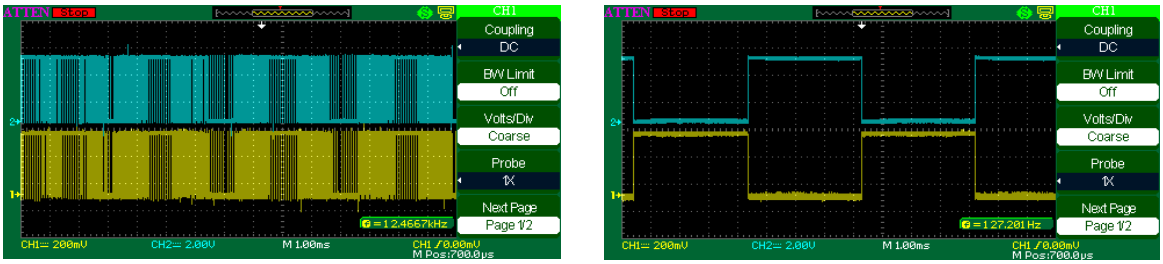
Table 2. Parameters of simulation and implementation

V_{in}	: 300 Volt DC
Capasitor	: 220 uF/450V
Inductor	: 2 mH, 5mH
Resistif Load	: 100 Ohm
Switching frequency	: 5 KHz, 20KHz



(a) (b)

Figure 5. Simulated waveforms: (a) Switching on S_1- S_2 (b) Switching on S_3-S_6, *and* S_4- S_5



(a) (b)

Figure 6. Implemented waveforms: (a) switching on S_1- S_2 (b) Switching on S_3-S_6, *and* S_4- S_5

Figure 5(a) and 6(a) show a sinusoidal pulse width modulation used to switch S_1 and S_2. Figure 5 (b) and 6(b) meanwhile show a pulse shaper polarity inverter at 50 Hz used to switch S_3-S_6 and S_4- S_5. In this strategy, the power switch S_1 and S_2 used a high switching frequency. For this reason the power switch that was used must have a high switching capability. Conversely the power switch on S_3-S_6 and S_4- S_5 can use the power switch with a low switching frequency.

Figure 7(a) shows the simulation result of five-level voltages of inverter outputs. The magnitude of the first, second, third, fourth, and fifth voltage levels were at +300V, +150V, 0V, -150V and -300V respectively; whereas to obtain the fundamental value of the filter inductor voltage has been used. Figure 7 (a) shows the significant value of the fundamental harmonic voltage. The magnitude of the voltage harmonics was related to the ripple current in Equation (9) and (10), enabling to minimize the voltage harmonics by enlarging the filter inductor (Figure 7(b)) or switching frequency (Figure 7(c)) or both of them (Figure 7 (d)), Figure 8 shows the implementation result of five-level voltages of inverter outputs

Figure 9 shows the simulation and implementation result of voltage in capacitor, the magnitude of the first, second, were at 150V. This control strategy is possible equilibrium voltage on the capacitor. Balancing the voltages of DC capacitors is very important in controlling the multilevel inverter. The voltage balance of DC capacitor voltages V_{C1} and V_{C2} can be controlled by the power electronic switches S_1 and S_2 easily using phase shifted carrier.

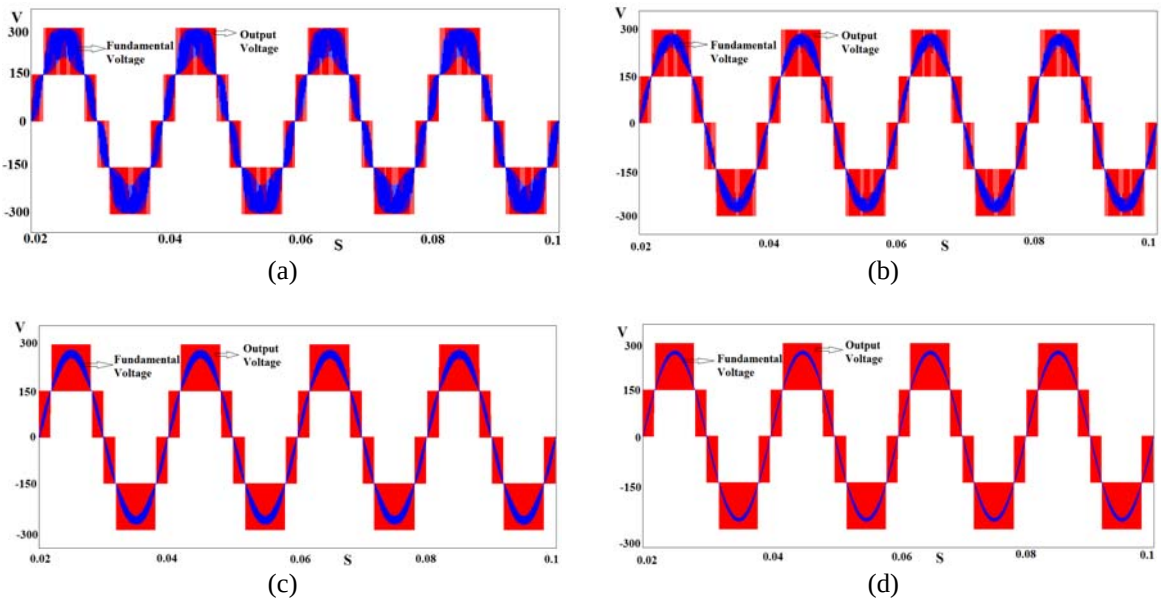


Figure 7. Simulated waveforms of output voltage: (a) f = 5KHz, L = 2mH (b) f = 5KHz, L = 5mH (c) f = 10KHz, L = 2mH (d) f = 10KHz, L = 5mH

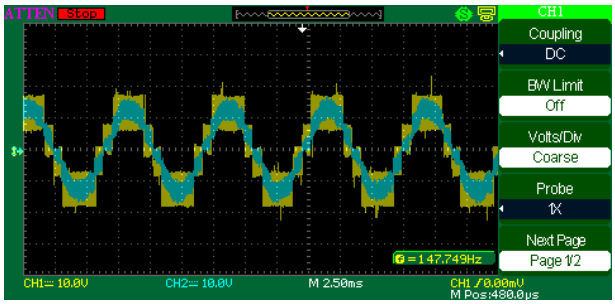


Figure 8. Implemented waveforms of output voltage: f = 5KHz, L = 2mH

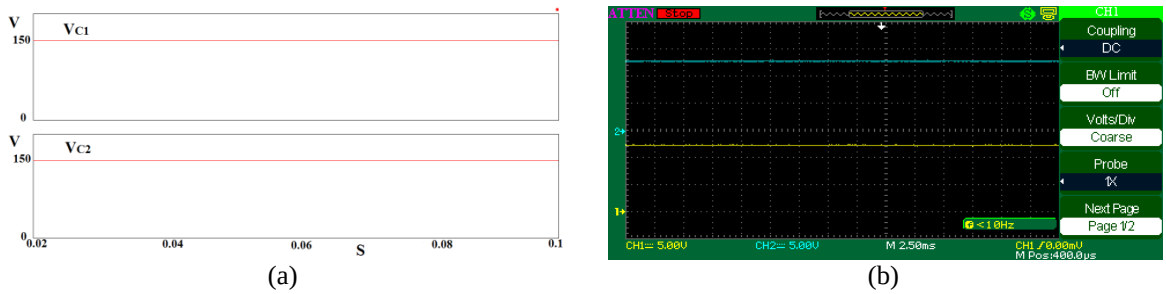


Figure 9. Capacitor voltage: (a) Simulated waveforms between the value of V_{c1} and V_{c2} (b) Implemented waveforms between the value of V_{c1} and V_{c2}

4. CONCLUSION

A proposed inverter topology has more advantages compared to the conventional one in terms of the equilibrium voltage on the capacitor, DC isolation, control requirements, cost, and reliability. It is shown that this topology can be a good candidate for converters used in power applications as in Photovoltaic systems, UPS, etc. In the mentioned topology, the switching operation was separated into high and low frequency parts. Pulse width modulation for the inverter had simplicity requiring no voltage balance in the capacitor. Further, the proposed topology can effectively work as a five-level inverter with a new carrier for modulation strategy.

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